ANNA UNIVERSITY, CHENNAI

NON- AUTONOMOUS COLLEGES

AFFILIATED TO ANNA UNIVERSITY

M.E. APPLIED ELECTRONICS

REGULATIONS 2025

PROGRAMME OUTCOMES (POs):

PO	Programme Outcomes
PO1	An ability to independently carry out research /investigation and development work to solve practical problems
PO2	An ability to write and present a substantial technical report/document.
PO3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

PROGRAMME SPECIFIC OUTCOMES(PSOs):

PSO	Programme Specific Outcomes
PSO1	Ability to design and implement innovative solutions to solve complex problems in Applied Electronics.
PSO2	Competence to independently undertake research projects involving simulation, measurement, and product development in Applied Electronics-related fields.

ANNA UNIVERSITY, CHENNAI

POST GRADUATE CURRICULUM (NON.AUTONOMOUS AFFILIATED INSTITUTIONS)

Programme: M.E., Applied Electronics **Regulations:** 2025

Abbreviations:

BS – Basic Science (Mathematics, Physics, Chemistry)
ES – Engineering Science (General (**G**), Programme Core (**PC**), Programme Elective (**PE**)
SD – Skill Development
SL – Self Learning
TCP – Total Contact Period(s)
L – Laboratory Course
T – Theory
LIT – Laboratory Integrated Theory
PW – Project Work

Semester I

S. No.	Course Code	Course Title	Type	Periods per week			TCP	Credits	Category
				L	T	P			
1.	MA25C05	Advanced Mathematical Methods (ECE)	T	4	0	0	4	4	BS
2.	AP25101	Statistical Signal Processing and Modeling	T	3	1	0	4	4	ES (PC)
3.	AP25C01	Advanced Digital System Design	T	3	1	0	4	4	ES (PC)
4.	AP25C02	Analog Integrated Circuit Design	T	3	0	0	3	3	ES (PC)
5.	AP25C03	Digital CMOS VLSI Design	T	3	0	0	3	3	ES (PC)
6.	AP25C04	Analog IC Design Laboratory	L	0	0	4	4	2	ES (PC)
7.	AP25102	Technical Seminar	-	0	0	2	2	1	SD
						Total	**24**	**21**	

Semester II

S. No.	Course Code	Course Title	Type	Periods per week			TCP	Credits	Category
				L	T	P			
1.	AP25201	Industrial Internet of Things	T	3	1	0	4	4	ES (PC)
2.	AP25202	High Speed Circuit Design	T	3	1	0	4	4	ES (PC)
3.		Programme Elective I	T	3	0	0	3	3	ES (PE)
4.	AP25203	Embedded System Design	LIT	3	0	2	5	4	ES (PC)
5.	-	Industry Oriented Course I	---	1	0	0	1	1	SD
6.	AP25204	Industrial Training	-	-	--	-	---	1	SD
7.	-	Self-Learning Course	-	-	--	-	---	1	--
						Total	**17**	**18**	

Semester III

S. No.	Course Code	Course Title	Type	Periods per week			TCP	Credits	Category
				L	T	P			
1.		Programme Elective II	T	3	0	0	3	3	ES (PE)
2.		Programme Elective III	T	3	0	0	3	3	ES (PE)
3.		Programme Elective IV	T	3	0	0	3	3	ES (PE)
4.	-	Programme Elective V	T	3	0	0	3	3	ES (PE)
5.	-	Industry Oriented Course II	---	1	0	0	1	1	SD
6.	AP25301	Project Work I	---	0	0	12	12	6	SD
						Total	**25**	**19**	

Semester IV

S. No.	Course Code	Course Title	Type	Periods per week			TCP	Credits	Category
				L	T	P			
1.	AP25401	Project Work II	---	0	0	24	24	12	SD
						Total Credits	**24**	**12**	

Programme Elective Courses (PE)

S. No.	Course Code	Course Title	Periods per week			Total Contact Periods	Credits
			L	T	P		
1.	VL25C03	Digital Image and Video Processing	3	0	0	3	3
2.	AP25001	DSP Architecture and Programming	3	0	0	3	3
3.	EL25C04	RF Integrated Circuit Design	3	0	0	3	3
4.	EL25C05	Electromagnetic Interference and Compatibility	3	0	0	3	3
5.	AP25002	Advanced Microprocessors and Microcontrollers Architectures	3	0	0	3	3
6.	AP25003	Advanced Computer Architecture Design	3	0	0	3	3
7.	AP25C05	Signal Integrity for High Speed Design	3	0	0	3	3
8.	AP25004	VLSI Interconnects	3	0	0	3	3
9.	AP25005	Semiconductor Memory Design	3	0	0	3	3
10.	AP25006	Algorithms For VLSI Physical Design Automation	3	0	0	3	3
11.	AP25007	Statistical Analysis and Optimization for VLSI	3	0	0	3	3
12.	AP25008	System on Chip Design	3	0	0	3	3
13.	AP25C06	Hardware /Software Co Design	3	0	0	3	3
14.	VL25C02	MEMS and NEMS	3	0	0	3	3
15.	EL25C01	Cryptography and Network Security	3	0	0	3	3
16.	AP25009	Neuromorphic Computing	3	0	0	3	3
17.	AP25010	Artificial Intelligence for Hardware Design	3	0	0	3	3
18.	AP25011	IP Core Design and Protection	3	0	0	3	3
19.	AP25012	Spintronics and Quantum Computing	3	0	0	3	3
20.	CU25C14	Analog and Mixed Signal VLSI Design	3	0	0	3	3

Semester I

MA25C05	Advanced Mathematical Methods (ECE)	L	T	P	C
		3	1	0	4

Course Objectives:

This course aims to equip students with advanced mathematical and computational techniques focuses on developing problem-solving skills for designing efficient circuits, communication protocols, and embedded systems.

Calculus of Variations: Variation and its properties, Euler's equation, Functionals dependent on first and higher order derivatives, Functionals dependent on functions of several independent variables, Some applications, Direct methods, Ritz method.

Queueing Models: Markovian queues, Birth and death processes, Single and multiple server queueing models, Little's formula, Queues with finite waiting rooms, Queues with impatient customers: Balking and reneging. Finite source models, M/G/1 queue, Pollaczek Khinchin formula, M/D/1 and M/EK/1 as special cases, Series queues, Open Jackson networks.

Graph Theory: Introduction to paths, trees, Isomorphism, Matrix coloring and directed graphs, Some basic algorithms: Dijkstra's Algorithm, Depth-First search, Breadth-First search, Prims Algorithm, Kruskal Algorithm

Optimization Techniques: Linear programming, Basic concepts, Graphical and simplex methods, Big M method, Transportation problems, Assignment problems.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Elsgolc, L. D. – *Calculus of Variations*, Dover Publications.
2. Gross, D. & Harris, C. M. – *Fundamentals of Queueing Theory*, Wiley.
3. Deo, N.–*Graph Theory with Applications to Engineering and Computer Science*, PHI.
4. Hillier, F. S. & Lieberman, G. J –*Introduction to Operations Research*, McGraw-Hill.
5. Kanti Swarup, Gupta P.K.,& Man Mohan–*OperationsResearch*, Sultan Chand &Sons.

E-resources:

1. https://nptel.ac.in/courses/111/105/111105039
2. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-262-discrete-stochastic-processes
3. https://nptel.ac.in/courses/106/106/106106183

AP25101	Statistical Signal Processing and Modeling	L	T	P	C
		3	1	0	4

Course Objectives:

To introduce random signal processing, modeling for prediction and estimation, spectral estimation (parametric & non-parametric), and MSE/adaptive filter design.

Introduction to Random Signal Processing: Discrete random processes, ensemble averages, stationarity, bias & estimation, autocovariance, autocorrelation, Parseval's theorem, Wiener-Khintchine relation, white noise, PSD, spectral factorization, filtering.

Activites: 1.Simulate discrete random processes in MATLAB/Python.
2. Compute ensemble averages, autocorrelation & PSD for sample signals

Signal Modeling: AR, MA, ARMA models, forward/backward linear prediction, Yule-Walker method, Prony's equations, Levinson-Durbin algorithm.

Activites: 1. Implement AR, MA, ARMA models using time-series data
2. Perform forward and backward prediction

Spectral Estimation: Spectral estimation from finite signals, nonparametric methods (periodogram, Bartlett, Welch, Blackman-Tukey), parametric methods, AR spectral estimation, harmonic detection.

Activites: 1. Apply periodogram, Bartlett, and Blackman-Tukey methods on signals
2. Detect harmonic components using AR spectral estimation

Linear Estimation: LMMSE filtering, Wiener-Hopf equations, FIR/IIR Wiener filters, causal/non-causal filters, noise cancellation.

Activites: 1. Design FIR and IIR Wiener filters in MATLAB/Python
2. Solve Wiener-Hopf equations for given signals

Adaptive Filters: FIR adaptive filters, steepest descent, LMS, normalized LMS, RLS algorithm, adaptive equalization, echo & noise cancellation.

Activites: 1. Implement LMS, Normalized LMS, and RLS algorithms
2. Compare convergence behavior of adaptive algorithms

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Hayes, M. H. (2002). Statistical digital signal processing and modeling. John Wiley & Sons, Inc.
2. Manolakis, D. G., & Ingle, V. K. (2011). Applied digital signal processing. Cambridge University Press.
3. Kay, S. M. (2017). Fundamentals of statistical signal processing: Estimation theory (Vol. 1),(vol 3) Detection theory (Vol. 2). Prentice Hall.
4. Kailath, T., Sayed, A. H., & Hassibi, B. (2000). Linear estimation. Prentice Hall.

	CO description	PO Mapping	PSO1	PSO2
CO1	Explain the concepts of random processes and their statistical properties.	-	-	-
CO2	Analyze signals using ARMA, AR, and MA models for prediction and analysis.	PO1(3) PO2(3)	3	3
CO3	Apply spectral estimation techniques to analyze signals in the frequency domain.	PO1(3) PO2(3)	2	2
CO4	Design and implement linear and adaptive filters for noise cancellation and signal enhancement.	PO1(3) PO3(3)	3	2

AP25C01	Advanced Digital System Design	L	T	P	C
		3	1	0	4

Course Objectives:

To study design and analysis of synchronous/asynchronous sequential circuits, PLD/ROM design, combinational/PLA testing, and Verilog HDL for digital system design.

Sequential Circuit Design: State diagrams/tables, state assignment & reduction, synchronous circuit design, iterative circuits, ASM charts.

Activities: 1. Design state diagrams for given problems
2. Implement synchronous circuits using ASM

Asynchronous Sequential Circuit Design: Flow table reduction, race conditions, hazards (static/dynamic/essential), mixed-mode circuits, vending machine controller design.

Activities: 1. Analyze and minimize flow tables
2.Identify and eliminate hazards

Fault Diagnosis and Testability Algorithms: Fault table, path sensitization, Boolean difference, D & Kohavi algorithms, PLA faults, DFT, BIST techniques.

Activities:1.Generate fault tables for combinational circuits
2. Simulate fault detection using D-algorithm

Synchronous Design Using Programmable Devices: PLD families, PLA/PAL-based circuit design, ROM design, FSM realization using PLDs, FPGA (Xilinx Vertex 7).

Activities:1. Iimplement FSM using PLA/PAL
2. Program and simulate FSM on FPGA

System Design Using Verilog: Verilog HDL modeling, data types, behavioral & structural modeling, FSM synthesis, test benches, combinational/sequential circuit realization.

Activities: 1. Write and simulate Verilog code for registers, counters, serial adders
2.Design and test a simple microprocessor in Verilog

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Arnold, M. G. (1999). *Verilog digital–computer design*. Prentice Hall PTR.
2. Biswas, N. N. (2001). *Logic design theory*. Prentice Hall of India.
3. Lala, P. K. (2015). *Digital system design using PLD* (Reprint ed.). B S Publications.
4. Lala, P. K. (2020). *Fault tolerant and fault testable hardware design*. B S Publications.
5. Palnitkar, S. (2003). *Verilog HDL: A guide to digital design and synthesis*. Pearson.
6. Roth, C. H., Jr. (2013). *Fundamentals of logic design* (7th ed.). Thomson Learning.

	CO description	PO	PSO1	PSO2
CO1	Explain the fundamentals of synchronous and asynchronous sequential circuits	-	-	-
CO2	Analyze and design sequential circuits using state diagrams and ASM charts.	PO1(3)	2	2
CO3	Apply fault diagnosis and testability algorithms to digital circuits.	PO1(3) PO2(3)	3	3
CO4	Develop and simulate digital systems using Verilog HDL and FPGA.	PO1(3) PO2(3)	2	2

AP25C02	Analog Integrated Circuit Design	L	T	P	C
		3	0	0	3

Course Objectives:
To Study single-stage amplifier design, high-frequency/noise characteristics, operational amplifiers, voltage/current reference circuits with practical exercises

Single Stage Amplifiers: MOS physics, equivalent circuits, CS, CG, source follower, differential & cascode amplifiers, design for SR, gain, BW, ICMR, power, voltage swing.
Activities:1. Design and simulate CS, CG amplifiers
2. Calculate gain, bandwidth, slew rate for given specification

High Frequency and Noise Characteristics of Amplifiers: Miller effect, pole analysis, frequency response of stages, noise sources, noise analysis in single stage and differential amplifiers.
Activities:1. Analyze frequency response using pole-zero plots
2. Simulate noise performance in amplifiers.

Negative Feedback Amplifiers and Operational Amplifiers: Feedback types, loading effects, op-amp parameters, one/two-stage op-amps, gain boosting, slew rate, PSRR, noise in op-amps.
Activities: 1.Design and simulate negative feedback circuits
2. Evaluate gain, slew rate, and PSRR of op-amps

Stability and Frequency Compensation of Two Stage Operational Amplifier: Two-stage op-amp analysis, phase margin, compensation methods, slew rate issues, advanced compensation techniques.

Activities:1. Analyze phase margin and stability in two-stage op-amps
2. Implement frequency compensation methods in simulations

Voltage and Current References: Current mirrors (Wilson, Widlar, Cascode), high swing cascode sinks, supply/temperature independent biasing, PTAT & CTAT currents, constant-Gm biasing.

Activities: 1. Design and simulate various current mirrors
2. Implement PTAT and CTAT current references

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References:

1. Allen, P. E., & Holberg, D. R. (2013). *CMOS analog circuit design* (3rd ed.). Oxford University Press.
2. Baker, R. J. (2019). *CMOS: Circuit design, layout, and simulation* (4th ed.). Wiley IEEE Press.
3. Grebene, A. B. (2003). *Bipolar and MOS analog integrated circuit design*. John Wiley & Sons.
4. Natarajan, A. (n.d.). *EE5390: Analog IC design* [Recorded lecture]. http://www.ee.iitm.ac.in/~ani/ee5390/index.html
5. Razavi, B. (2016). *Design of analog CMOS integrated circuits* (2nd ed.). Tata McGraw Hill.
6. Sansen, W. M. C. (2007). *Analog design essentials*. Springer.

	CO description	PO Mapping	PSO1	PSO2
CO1	Explain the theory and design concepts of analog circuits .	-	-	-
CO2	Analyse and design single-stage and multi-stage amplifiers considering high-frequency and noise characteristics to meet specified performance criteria.	PO1(3)	2	2
CO3	Apply concepts of negative feedback, stability, and frequency compensation in the design and analysis of operational amplifiers.	PO1(3) PO2(3)	3	3
CO4	Design and simulate voltage and current reference circuits with temperature and supply independence for analog integrated systems.	PO1(3) PO2(3)	2	2

AP25C03	Digital CMOS VLSI Design	L	T	P	C
		3	0	0	3

Course Objectives:

To Understand CMOS basics and design combinational/sequential circuits; apply structured VLSI design through case studies.

MOS Transistors and CMOS Inverter: MOS transistor characteristics, short channel effects, CMOS inverter design, stick diagrams, power, delay, sizing.
Activities:1. Simulate CMOS inverter characteristics and sizing effects
2. Draw stick diagrams and analyze power-delay trade

CMOS, Combinational Circuits: Complementary CMOS, power reduction, ratioed logic, pass transistor logic, dynamic CMOS, Domino, NP-CMOS.
Activities:1. Design combinational logic using different CMOS styles
2. Analyze power and switching activity in logic gates

CMOS, Sequential Circuits: Latches vs registers, flip-flops, dynamic/static registers, clocking strategies, Schmitt trigger, mono/astable circuits.

Activities:1. Implement various flip-flops and compare timing behavior
2. Design clocking schemes for latch/register pipelines

CMOS Sub System Design Adders (carry bypass, select, CLA), multipliers, counters, parity generators, multiplexers, shifters, memory elements.

Activities:1. Design fast adders and multipliers
2. Build and simulate small subsystems (e.g., counter + MUX)

Performance Estimation & Design Techniques:Delay estimation, logical effort, sizing, power, interconnects, scaling, synchronous and self-timed design.

Activities:1. Estimate delay and power for sample circuits
2. Compare synchronous vs self-timed circuit design .

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References

1. Weste, N. H. E., & Harris, D. (2011). *CMOS VLSI design: A circuits and systems perspective*. Pearson.
2. Rabaey, J. M., Chandrakasan, A., & Nikolić, B. (2003). *Digital integrated circuits*. Pearson.
3. Martin, K. (2011). *Digital integrated circuit design*. Oxford University Press.
4. Palnitkar, S. (2003). *Verilog HDL* (2nd ed.). Pearson Education.

	CO description	PO	PSO1	PSO2
CO1	Explain CMOS basics in digital circuits.	-	-	-
CO2	Analyze and design CMOS-based combinational and sequential circuits	PO1(3)	2	2
CO3	Apply various CMOS logic styles and techniques to optimize digital subsystems	PO1(3) PO2(3)	3	3
CO4	Evaluate and estimate circuit performance using structured approaches for subsystem design.	PO1(3) PO2(3)	2	2

AP25C04	Analog IC Design Laboratory	L	T	P	C
		0	0	4	2

Course Objectives:

To Design analog circuits from transistor level to IA implementation using CAD tools for simulation, layout, LVS, and parasitic extraction.

List of Experiments

1. Extraction of process parameters of CMOS process transistors
   a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
   b. Plot ID vs. VGS at particular drain voltage for NMOS, PMOS and determine Vt.
   c. Plot log ID vs. VGS at particular gate voltage for NMOS, PMOS and determine IOFF and sub- threshold slope.
   d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage To extract Vth use the following procedure.
      i. Plot gm vs VGS using SPICE and obtain peak gm point.
      ii. Plot y=ID/(gm) as a function of VGS using SPICE.
      iii. Use SPICE to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
   f. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.
2. CMOS inverter design and performance analysis
   a. i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
      ii. Plot VTC for CMOS inverter with varying VDD.
      iii. Plot VTC for CMOS inverter with varying device ratio.
   b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay tpHL, tpLH, 20%-to-80% rise time tr and 80%-to-20% fall time tf.
   c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.
3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.
4. Single stage amplifier design and performance analysis
   a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
   b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
      i. Establish a test bench to achieve VDSQ=VDD/2.
      ii. Calculate input bias voltage for a given bias current.

iii. Use spice and obtain the bias current. Compare with the theoretical value
iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
v. using small signal analysis in spice, considering load capacitance.
vi. Plot step response of the amplifier with a specific input pulse amplitude.
vii. Derive time constant of the output and compare it with the time constant
viii. resulted from -3dB Band Width.
ix. Use spice to determine input voltage range of the amplifier

5. Three OPAMP Instrumentation Amplifier (INA).
Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
i. Draw the schematic of OPAMP macro model.
ii. Draw the schematic of INA.
iii. Obtain parameters of the OPAMP macro model such that it meets a given specification for: i.low-frequency voltage gain, ii. unity gain BW (fu), iii.input capacitance, iv.output resistance, v.CMRR
a. Draw schematic diagram of CMRR simulation setup.
b. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
c. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
d. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6.Use Layout editor.
a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters.
b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
c. Extract the netlist. Use extracted netlist and obtain tPHLtPLH for the inverter using Spice.
d. Use a specific interconnect length and connect and connect three inverters in a chain.
e. Extract the new netlist and obtain tPHL and tPLH of the middle inverter.
f. Compare new values of delay times with corresponding values obtained in part ‘c’.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
a. low-frequency voltage gain,
b. unity gain BW (fu),
c. Power dissipation
i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
ii. Perform time domain simulation and verify low frequency gain.
iii. Perform AC analysis and verify.

Weightage: Continuous Assessment: 60%, End Semester Examinations: 40%
Assessment Methodology: Project (30%), Assignment (10%), Practical (30%), Internal Examinations (30%)

	CO description	PO	PSO1	PSO2
CO1	Characterize MOS transistors and design basic analog building blocks using simulation tools.	PO1(3)	2	2
CO2	Implement and simulate analog circuits through schematic entry, layout design, LVS, and parasitic extraction.	PO1(3) PO2(3)	3	3
CO3	Design and validate an instrumentation amplifier using a structured analog design flow with CAD tools.	PO1(3) PO2(3)	2	2

Semester II

AP25201	Industrial Internet of Things	L	T	P	C
		3	1	0	4

Course Objectives:

The objective of this course is to provide knowledge about IoT Nodes & Sensors, IoT Gateways, IoT Cloud Systems, IoT Cloud Dashboards and Challenges in IoT system Design.

Understanding IOT Concept and Development Platform

IOT Definition, Importance of IoT, Applications of IOT, IoT architecture, Understanding working of Sensors, Actuators, Sensor calibration, Study of Different sensors and their characteristics.

Activity 1: Exploring IoT Architecture Using a Real-World Scenario

Activity 2: Sensor Study and Calibration Experiment

Analysing & Decoding of Communication Protocol Used in IOT Development Platform

UART Communication Protocol, I2C Protocol device interfacing and decoding of signal, SPI Protocol device interfacing and decoding of signal, WIFI and Router interfacing, Ethernet Configuration, Bluetooth study and analysis of data flow, Zigbee Interfacing and study of signal flow.

Activity 1: Protocol Signal Analysis Using Logic Analyzer (UART, I2C, SPI)

Activity 2: Wireless Communication & Network Interface Study (WiFi, Ethernet, Bluetooth, Zigbee)

IOT Physical Devices and Endpoints and Controlling Hardware and Sensors

IoT Physical Devices and Endpoints- Introduction to Arduino and Raspberry Pi- Installation, Interfaces (serial, SPI, I2C), Programming – Python program with Raspberry PI with focus on interfacing external gadgets, controlling output, reading input from pins. Controlling Hardware- Connecting LED, Buzzer, Switching High Power devices with transistors, Controlling AC Power devices with Relays, Controlling servo motor, speed control of DC Motor, unipolar and bipolar Stepper motors; Sensors- Light sensor, temperature sensor with thermistor, voltage sensor, ADC and DAC, Temperature and Humidity Sensor DHT11, Motion Detection Sensors, Wireless Bluetooth Sensors, Level Sensors, USB Sensors, Embedded Sensors, Distance Measurement with ultrasound sensor.

Activity 1: Interfacing Physical IoT Devices (Arduino & Raspberry Pi) and Reading Sensors

Activity 2: Controlling Hardware Outputs (LED, Buzzer, Motors, Relays)

Cloud Services Used in IOT Development Platform

Configuration of the cloud platform, Sending data from the IOT nodes to the gateways using different communication options; Transferring data from gateway to the cloud; Exploring the web services like mail, Messaging (SMS) and Twitter etc.; Tracking of cloud data as per the requirement; Google Cloud service architect; AWS clod Services architect; Microsoft Azure cloud services Architect; OEN source Cloud Services; Initial State IoT Dashboard & Cloud Services

Activity 1: IoT Data Upload to Cloud Using Node–Gateway–Cloud Architecture

Activity 2: Exploring Multiple Cloud Architectures (AWS, Google, Azure, Open-Source) & Creating a Dashboard

Challenges in IOT System Design – Hardware & Software

Antenna design and placement, Chip-package system development, Power electronics, electromagnetic interference/compatibility (EMI/EMC), Electronics reliability; Battery simulation.

Activity 1: Practical Analysis of Hardware Challenges in IoT Design

Activity 2: Software Challenges & Battery Simulation for IoT Systems

References:

1. Bahga, A., & Madisetti, V. (2015). *Internet of things: A hands-on approach*. Universities Press. https://doi.org/9788173719547
2. Richardson, M., & Wallace, S. (2014). *Getting started with Raspberry Pi*. O'Reilly (SPD). https://doi.org/9789350239759
3. Monk, S. (2016). *Raspberry Pi cookbook: Software and hardware problems and solutions*. O'Reilly (SPD). https://doi.org/9789352133895
4. Ida, N. (2014). *Sensors, actuators and their interfaces*. SciTech Publishers.
5. Waher, P. (2015). *Learning Internet of Things*. Packt Publishing.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand IoT concepts, architecture, sensors, actuators, and development platforms	-	-	-
CO2	Analyze and decode communication protocols like UART, I2C, SPI, WiFi, Bluetooth, and Zigbee	PO2(3), PO3(3), PO4(2)	3	3
CO3	Interface and control IoT physical devices, sensors, and actuators using platforms like Arduino and Raspberry Pi	PO3(3), PO4(3), PO5(2)	3	3
CO4	Use cloud platforms for IoT data management, dashboard creation, and real-time monitoring	PO3(3), PO4(3), PO6(2)	3	3
CO5	Identify and address hardware and software challenges in IoT system design, including EMI/EMC and power considerations	PO3(3), PO4(3), PO6(2)	3	3

AP25202	High Speed Circuit Design	L	T	P	C
		3	1	0	4

Course Objectives:

The objective of this course is to introduce the basics of PCB design and high speed PCB design techniques. It also aims to provide hands-on experience on PCB design with CAD tools.

Basics of PCB Design, Tools & Industry Standards

Printed Circuit Board Fabrication- PCB cores and layer stack-up. PCB fabrication process- Photolithography and chemical etching, Mechanical milling and Layer registration. Function of the Layout in the PCB Design Process. Design Files Created by Layout - Layout format files, Postprocess (Gerber) files, PCB assembly layers and files. Introduction to the Standards Organizations, Classes and Types of PCBs, Introduction to Standard Fabrication Allowances, PCB Dimensions and Tolerances, Copper Trace and Etching Tolerances, Standard Hole Dimensions, Soldermask Tolerance.

Activity 1: PCB Layout Creation & Gerber File Generation

Activity 2: PCB Fabrication & Industry Standards Study

PCB Design Flow Using CAD Tool

Overview of Computer-Aided Design. Setting up the user account, Starting a new project, Schematic Entry, Placing and wiring (connecting) the parts, Converting Schematic to Layout, Layout Environment and Tool Set, Designing the PCB with Layout – Setting constraints, Placing the parts, Auto routing and the Manual routing, Performing a design rule check, Making a board outline, Post processing the board design for manufacturing, Submitting Gerber files and requesting a quote, Annotating the layer types and stack-up, Receipt inspection and testing, Nonstandard Gerber files.

Activity 1: Complete PCB Design Flow Using a CAD Tool (KiCad / EasyEDA / Eagle / Altium)

Activity 2: PCB Validation, Inspection & Understanding Industry Requirements

Design Constraints for Manufacturing

PCB Assembly and Soldering Processes- Component Placement and Orientation Guide, Component Spacing for Through-hole Devices (THDs). Component Spacing for Surface Mounted Devices (SMDs), Mixed THD and SMD Spacing Requirements. Footprint and Pad stack Design for PCB Manufacturability- Land Patterns for SMDs- Land Patterns for THDs, Pad stack design, Hole-to-lead ratio, PTH land dimension (annular ring width), Clearance between plane layers and PTHs Solder mask and solder paste dimensions.

Activity 1: Component Placement & Spacing Analysis for PCB Manufacturability

Activity 2: Footprint, Padstack & Solder Mask/Paste Design for Manufacturing

High Speed PCB Design

Introduction to High-Speed PCB Design, Signal Integrity for PCB Designers, Causes of Signal Integrity Issues in a PCB, PCB Transmission Lines and Controlled Impedance, Electromagnetic Compatibility (EMC), Power Integrity

Activity 1: Signal Integrity & Transmission Line Analysis on a High-Speed PCB

Activity 2: EMC/EMI & Power Integrity Design Evaluation

High Speed PCB Stackup Design & PCB Technology

PCB Stackup Design, Terms and Definitions for Stackup, Selecting High-Speed Materials, Effect of Different Styles of Fibreglass Weaves on Impedance,

Activity 1: PCB Stackup Design and Material Selection

Activity 2: Effect of Fiberglass Weave on Impedance

High-Speed PCB Layout Design

Footprint Design for High-Speed Boards, Component Placement, High-Speed Routing Strategy, Vias and Microvias

Activity 1: Footprint Design and Component Placement for High-Speed Boards

Activity 2: High-Speed Routing Strategy with Vias and Microvias

References:

1. Mitzner, K. (2009). *Complete PCB design using OrCAD Capture and Layout* (1st ed.). Newnes.
2. Monk, S. (2017). *Make your own PCBs with EAGLE: From schematic design to finished boards* (2nd ed.). McGraw-Hill Education TAB.
3. Sierra Circuits Inc. (2020). *High-speed PCB design guide*.
4. Brooks, D. (2012). *Signal integrity issues and printed circuit board design*. Prentice Hall PTR.
5. Ritchey, L. W., Zasio, J., & Knack, K. J. (2003). *Right the first time: A practical handbook on high-speed PCB and system design*. Speeding Edge.
6. COEP Virtual Labs. (n.d.). *PCB design and fabrication*.
7. https://fab-coep.vlabs.ac.in/exp/pcb-design-fabrication/
8. NPTEL. (n.d.). *PCB design online course*. https://onlinecourses.nptel.ac.in/noc24_ee127/preview

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand the basics of PCB design, fabrication, layers, standards, tolerances, and design files	-	-	-
CO2	Apply CAD tools for PCB design, schematic entry, layout creation, auto/manual routing, and DRC	PO3(3), PO4(3), PO5(2)	3	3
CO3	Design PCB considering manufacturability constraints including component spacing, padstack, and soldermask	PO3(3), PO4(3), PO5(2)	3	3
CO4	Analyze high-speed PCB design considerations including signal integrity, EMC/EMI, transmission lines, and power integrity	PO3(3), PO4(3), PO6(2)	3	3
CO5	Design and optimize high-speed PCB stackups, material selection, component placement, and routing strategies including vias and microvias	PO3(3), PO4(3), PO5(2)	3	3

AP25203	Embedded System Design	L	T	P	C
		3	0	2	4

Course Objectives:

- To understand the design, development, and optimization of embedded computing systems, including hardware, software, and distributed architectures.
- To apply embedded system concepts and ARM processor programming to real-world applications through case studies and system design projects.

Embedded Computing Platform – Hardware Aspect

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process - CPU: Programming input and output CPU performance – CPU power consumption- CPU buses – Memory devices – Input / Output devices – Component interfacing- Designing with microprocessor development and debugging.

Activity 1: Microprocessor I/O Interfacing

Activity 2: CPU Performance and Power Measurement

Distributed Embedded Computing Platform

Multiprocessors- CPUs and Accelerators – Performance Analysis- Distributed Embedded Architecture – Networks for Embedded Systems: - I^2C Bus, CAN Bus, SHARC Link Port-Ethernet, Myrinet – Network based design – Internet enabled systems-Network based system performance Analysis

Activity 1: Network Communication in Embedded Systems

Activity 2: Performance Analysis of Multiprocessor Systems

ARM Processor

ARM Processor Fundamentals- ARM Cortex M3 Processor Architecture- MBED NXP LPC1768 – Pinout Details and Peripherals-ARM Assembly Language Instruction Set-Addressing Modes- Programming.

Activity 1: Exploring ARM Cortex-M3 Architecture

Activity 2: ARM Assembly Language Programming

System Design – Application Case Study

Design Models, Quality Assurance, Design Example: Toy Train Controller, Digital Alarm Clock, Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Box.

Activity 1: Embedded System Design Case Study

Activity 2: Hardware-Software Co-Design Exercise

Practical Exercises:

1. Push button, LED, LCD display and RTC interfacing with AVR RISC based microcontroller.
2. AVR RISC based Microcontroller system design with Touch screen interfacing.
3. Motor (DC, stepper, servo) interfacing with AVR RISC based Microcontroller.
4. Interfacing sensors and RFID with AVR RISC based Microcontroller.
5. Design of RC5 remote control decoder with AVR RISC based Microcontroller.
6. Implementing I2C, SPI, CAN and UART protocols with ARM 7 processor.
7. Design and implementation of path tracking and obstacle avoidance Robot.
8. Design and implementation of self-balancing Robot.
9. Design and implementation of Robotic Arm manipulation with 6 DOF.
10. Design and implementation of Pick and Place robot.

11. Design and implementation of color and pattern guided material handling robot.
12. Design and implementation of human detection robot using PIR sensor.

References:

1. Wolf, W. (2012). *Computers as components: Principles of embedded computing system design* (3rd ed.). Morgan Kaufmann Publishers.
2. Sloss, A. N., Symes, D., & Wright, C. (2008). *ARM system developer's guide: Designing and optimizing system software*. Elsevier/Morgan Kaufmann.
3. Elahi, A., & Arjeski, T. (2015). *ARM assembly language with hardware experiments*. Springer.
4. Liu, J. W. S. (2001). *Real-time systems*. Pearson Education Asia.
5. Krishna, C. M., & Shin, K. G. (2017). *Real-time systems* (1st ed., reprint). McGraw-Hill.
6. Vahid, F., & Givargis, T. (2006). *Embedded system design: A unified hardware/software introduction*. John Wiley & Sons.

Weightage: Continuous Assessment: 50%, End Semester Examinations: 50%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand the design, development, and optimization of embedded computing platforms including CPU, memory, buses, and I/O devices	-	-	-
CO2	Apply distributed embedded computing concepts, multiprocessor architectures, and communication protocols (I2C, CAN, Ethernet)	PO3(3), PO4(3), PO5(2)	3	3
CO3	Understand ARM processor fundamentals, architecture, instruction set, and peripherals	PO1(3), PO2(2), PO3(2)	3	2
CO4	Design embedded system applications using hardware-software co-design approaches and case studies	PO3(3), PO4(3), PO5(2)	3	3
CO5	Implement practical embedded system projects including interfacing sensors, motors, displays, communication protocols, and robotic systems	PO3(3), PO4(3), PO6(2)	3	3

Programme Elective Courses

VL25C03	Digital Image and Video Processing	L	T	P	C
		3	0	0	3

Course Objectives:

This course aims to provide an in-depth understanding of advanced concepts in digital image and video processing, with a strong focus on temporal analysis, motion estimation, and 3D reconstruction. Students will learn to apply state-of-the-art techniques in video compression, tracking, and deep learning-based analysis to solve real-world problems. By the end of the course, learners will be equipped to design and implement efficient image and video processing systems for applications such as surveillance, autonomous systems, and immersive media.

Motion Estimation and Video Fundamentals

Temporal vs. spatial image processing - Basics of video formation and representation (color video, interlaced vs. progressive) - Frame differencing and background subtraction - Block matching algorithms (Full Search, Three Step Search, Diamond Search) - Optical flow (Lucas-Kanade and Horn-Schunck methods) - Applications: surveillance, object tracking.

Activity 1: Motion Estimation with OpenCV (Block Matching vs. Optical Flow) - Tools: OpenCV (Python), sample videos (e.g., from UCF101 dataset) - Task: Implement and compare block matching and optical flow algorithms (Lucas-Kanade & Farnebäck) on test videos. - Outcome: Analyze tracking performance under different motion types.

Activity 2: Flipped Class + Mini Project on Background Subtraction Techniques - Tools: OpenCV, Code samples from GitHub - Task: Pre-class video lectures + in-class implementation of MOG2 and KNN background subtraction on surveillance footage. - Outcome: Comparative report and demonstration of real-time performance.

Video Compression Standards and Techniques

Temporal redundancy and inter-frame coding - Overview of video compression standards: MPEG-1/2/4, H.264/AVC, HEVC - Intra vs. inter coding, GOP structure - Motion compensation and entropy coding in video codecs - Scalable and Multiview video coding.

Activity 1: Video Codec Analysis using FFmpeg - Tools: FFmpeg (open source), sample videos from Xiph.org Video Test Media - Task: Encode videos using H.264, MPEG-4, and HEVC. Evaluate size, PSNR, and SSIM. - Outcome: Compression efficiency report.

Activity 2: Flipped Classroom on GOP Structure - Tools: Handbrake + OpenCV + Python - Task: Analyze Group of Pictures (GOP) in compressed video streams. - Outcome: Presentation on impact of GOP length and I/P/B frame configuration.

3D Image Processing and Multiview Video

Stereoscopic imaging and disparity map estimation - 3D reconstruction from multiple images - Structure from motion (SfM) - Multiview video systems and depth estimation - Applications in VR/AR and 3D television.

Activity 1: Stereo Vision and Disparity Map Generation - Tools: OpenCV stereo block matching, Middlebury Stereo Dataset - Task: Compute disparity maps from stereo pairs and visualize depth. - Outcome: Depth map quality evaluation and report.

Activity 2: Structure from Motion (SfM) using COLMAP - Tools: COLMAP (open source SfM), ETH3D dataset - Task: Reconstruct sparse and dense 3D scenes from multiple views. - Outcome: 3D point cloud visualization and reconstruction accuracy analysis.

Advanced Image and Video Analysis

Video segmentation and object tracking (Kalman filter, mean-shift, particle filter) - Action and gesture recognition - Scene understanding and semantic segmentation - Face and emotion recognition in video - Deep learning applications: CNNs for video, 3D CNNs, RNNs/LSTMs.

Activity 1: Action Recognition using Pre-trained CNN-LSTM Models Tools: PyTorch or TensorFlow, UCF101 dataset - Task: Use pretrained 3D CNN + LSTM pipeline to classify video actions. - Outcome: Confusion matrix + model performance summary.

Activity 2: Seminar on Research Paper Reproduction - Task: Reproduce a recent CVPR/ICCV paper (e.g., Deep SORT, YOLOv7 tracking) using open-source codebases. - Outcome: Present implementation steps, results, and challenges faced.

Real-Time Processing and Applications

Real-time image/video processing architectures (GPU, FPGA) - Edge AI and deployment on embedded devices - High-speed video capture and analysis - Applications: autonomous driving, medical video analysis, drone surveillance - Case studies and open research challenges.

Activity 1: Real-Time Object Tracking using Jetson Nano / Raspberry Pi - Tools: OpenCV + YOLOv5 or MobileNet-SSD, webcam or real-world video - Task: Deploy real-time object tracker on edge device. - Outcome: Demonstrate live tracking with FPS metrics.

Activity 2: Industry Case Study + Application Prototype - Task: Case study discussion on a real-world use (e.g., medical video analysis or drone surveillance) + student prototype. - Tools: Custom project using open-source libraries (e.g., OpenMMLab) - Outcome: Presentation + demo + report.

References

1. Szeliski, R. (2022). *Computer vision: Algorithms and applications* (2nd ed.). Springer.
2. Bovik, A. C. (Ed.). (2020). *The essential guide to video processing* (2nd ed.). Academic Press.
3. Singh, R. (2023). *Digital image and video processing: Principles and algorithms* (1st ed.). McGraw-Hill Education.
4. Marques, O. (2019). *Practical image and video processing using MATLAB* (2nd ed.). Wiley.
5. Goodfellow, I., Bengio, Y., & Courville, A. (2021). *Deep learning* (2nd ed.). MIT Press.

E-Resources

1. NPTEL Course: Digital Image Processing by Prof. P.K. Biswas, IIT Kharagpur.
2. NPTEL Course: Computer Vision by Prof. S. Raman, IIT Gandhinagar.
3. OpenCV Tutorials: https://docs.opencv.org/4.x/d6/d00/tutorial_py_root.html.
4. Coursera Course: Applied Computer Vision with Deep Learning (DeepLearning.AI).
5. CMU Video Lectures: Computer Vision (16-720) on YouTube.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Analyze the temporal characteristics of video sequences and apply motion estimation techniques such as block matching and optical flow to detect and track motion.	-	-	-
CO2	Evaluate and implement modern video compression algorithms by evaluating temporal and spatial redundancies for efficient video coding.	PO3(3)	3	1
CO3	Create depth maps and perform 3D reconstruction from stereo or Multiview image sequences using structure-from-motion techniques.	PO1(3)	3	1
CO4	Apply machine learning and deep learning models to recognize actions, objects, and scenes in video sequences with temporal consistency.	PO1(3) PO(2)	2	3

AP25001	DSP Processor Architecture and Programming	L	T	P	C
		3	0	0	3

Course Objective:

The objective of this course is to provide in-depth knowledge on Digital Signal Processors, DSP Architecture and programming skills, Advanced DSP architectures and applications.

Fundamentals of Programmable DSPs

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

TMS320C5X Processor

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

TMS320C6X Processor

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

ADSP Processors

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

Advanced Processors

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

Activities:

1. Quiz for each module
2. Read the data sheets of the processors studied and compare their features.

References:

1. Singh, A., & Srinivasan, S. (2012). *Digital signal processing: Implementations using DSP microprocessors with examples from TMS320C54xx*. Cengage Learning India Private Limited.
2. Venkataramani, B., & Bhaskar, M. (2003). *Digital signal processors: Architecture, programming and applications*. Tata McGraw-Hill Publishing Company Limited.
3. Chassaing, R. (2005). *Digital signal processing and applications with the C6713 and C6416 DSK*. John Wiley & Sons.
4. Texas Instruments, Analog Devices, & Motorola. (n.d.). *User guides*.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%
Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand fundamentals of programmable DSPs, including multiplier structures, memory access, VLIW architecture, pipelining, and addressing modes	-	-	-
CO2	Analyze the architecture and instruction set of TMS320C5X processor and write assembly language programs for real-time signal processing	PO3(3), PO4(3), PO5(2)	3	3
CO3	Understand TMS320C6X architecture, development tools, programming, and real-time DSP application implementation	PO3(3), PO4(3), PO5(2)	3	3
CO4	Analyze ADSP-21XX and ADSP-210XX processor architectures, addressing modes, assembly instructions, and DSP application programs	PO3(3), PO4(3), PO5(2)	3	3

EL25C04	RF Integrated Circuit Design	L	T	P	C
		3	0	0	3

Course Objectives:

To study CMOS transceiver design, noise analysis, impedance matching, amplifier and feedback system design, mixers, oscillators, and frequency synthesizers for high-performance communication systems.

CMOS Physics, Transceiver Specifications and Architectures

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter**.**

Activity: Analysis of CMOS Transceiver Architectures and Noise Performance in Communication Systems

Impedance Matching and Amplifiers

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

Activity: Design and Analyze a Source-Degenerated Common-Source LNA Using S-Parameters and Smith Chart–Based Impedance Matching

Feedback Systems and Power Amplifiers

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model — Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

Activity: Analyze Stability, Efficiency, and Linearity in Class A–F Power Amplifiers Using Gain/Phase Margin, Root-Locus, and ACPR Evaluation

Mixers and Oscillators

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

Activity: Analyze and Compare Mixer Architectures and Oscillator Designs Using Nonlinear Characteristics, Describing Functions, and Phase-Noise Evaluation

PLL and Frequency Synthesizers
Linearized Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

Activity: Model and Evaluate a PLL-Based Integer-N Frequency Synthesizer Using Linearized Loop Analysis, Noise Characterization, and Phase-Detector/Charge-Pump Design

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References

1. Lee, T. (2004). Design of CMOS RF integrated circuits. Cambridge University Press.
2. Razavi, B. (2013). RF microelectronics (2nd ed.). Pearson Education.
3. Crols, J., & Steyaert, M. (1997). CMOS wireless transceiver design. Kluwer Academic Publishers.
4. Razavi, B. (2017). Design of analog CMOS integrated circuits (2nd ed.). McGraw-Hill Education.
5. Indian Institute of Technology Madras. (n.d.). EE6240 – Recorded lectures and notes. http://www.ee.iitm.ac.in/~ani/ee6240/

	CO description	PO Mapping	PSO1	PSO2
CO1	understand user specifications for RF systems	-	-	-
CO2	design RF low noise amplifiers,power amplifiers,RF mixers and oscillators	PO3(3)	3	2
CO3	Analyze PLL for RF applications	PO1(3)	3	2

EL25C05	Electromagnetic Interference and Compatibility	L	T	P	C
		3	0	0	3

Course Objective:

This course aims to equip students with a comprehensive understanding of Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC), enabling them to identify and analyze EMI sources and coupling mechanisms, apply effective mitigation techniques like shielding, grounding, and filtering, comprehend relevant national and international EMC standards and regulations, and gain practical knowledge of EMI/EMC test methods and instrumentation, ultimately allowing them to design electromagnetically compatible electronic systems and PCBs.

Introduction to EMI & EMC

Definitions and Concepts – EMC Environment - EMC Testing Categories - Basic Electromagnetic Theory: Maxwell's equations and their application in EMC, Near-field and far-field approximations, Concepts of impedance

Activity 1: EMI Source Identification & Classification
Activity 2: Near-Field vs Far-Field Exploration Using Simple Calculations

EMI Coupling Mechanisms

Coupling Paths - basic coupling mechanisms: Conducted Coupling, Capacitive Coupling, Inductive/Magnetic Coupling, Radiative / Electromagnetic Coupling – Crosstalk - Transient Sources - Automotive transients.

Activity 1: Identify and Classify EMI Coupling Mechanisms in Real Devices
Activity 2: Hands-On Demonstration of Crosstalk and Transient Effects

EMI Mitigation Techniques & EMC Standards

Shielding – Grounding – Filtering – Cabling – Bonding - Need for Standards - National and International EMC Standardizing Organizations: IEC, FCC, CISPR, ANSI, BSI, CENELEC, ETSI - Key Standards and Specifications: MIL-STD, Electro Magnetic Emission and Susceptibility standards.
Activity 1: EMI Mitigation Hands-On Experiment
Activity 2: EMC Standards Research & Presentation

EMI Test Methods and Instrumentation

Fundamental Considerations - Emission Testing: Conducted Emissions, Radiated Emissions - Immunity/Susceptibility Testing: Conducted Immunity, Radiated Immunity, ESD Testing, Transient Immunity - Test Equipment
Activity 1: Emission Testing Demonstration
Activity 2: Immunity and ESD Testing Simulation

PCB Design for EMC Compliance

PCB Layout and Stack-up - Signal Integrity Considerations - Mixed-Signal PCB Layout: Grounding and power distribution for mixed-signal systems, Isolation of sensitive circuits - Component Placement for EMC
Activity 1: Analyzing PCB Layout for EMC Issues
Activity 2: Design a Simple EMC-Compliant PCB Section

References:

1. Ott, H. W. (1988). *Electromagnetic compatibility engineering* (2nd ed.). John Wiley & Sons.
2. Paul, C. R. (2010). *Introduction to electromagnetic compatibility* (2nd ed.). Wiley Interscience.
3. Ott, H. W. (1988). *Noise reduction techniques in electronic systems* (2nd ed.). John Wiley & Sons.
4. Keiser, B. (1989). *Principles of electromagnetic compatibility* (3rd ed.). Artech House.
5. Kodali, V. P. (2001). *Engineering electromagnetic compatibility: Principles, measurements, and technologies with computer models* (2nd ed.). IEEE Press.

E-Resources:

1. http:// www.ewh.ieee.org/soc/emcs/
2. https://archive.nptel.ac.in/courses/108/106/108106138/
3. https://nptel.ac.in/courses/108106138
4. https://onlinecourses.nptel.ac.in/noc24_ee67/preview

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Identify, categorize, and explain various sources of electromagnetic interference and EMC testing categories and EMI/EMC test methods, recognize the associated instrumentation, and critically evaluate test results for compliance.	-	-	-
CO2	Analyze and classify the coupling mechanisms (conducted, radiated, capacitive, inductive), and their impact on electronic systems.	PO3(3)	2	3
CO3	Integrate EMC principles into the design process of electronic circuits and printed circuit boards (PCBs), optimizing layouts, component placement, and power/ground distribution to ensure inherent electromagnetic compatibility.	PO1(3) PO(2)	2	3

AP25002	Advanced Microprocessors and Microcontrollers Architectures	L	T	P	C
		3	0	0	3

Course Objectives:

This course aims to expose the students to the fundamentals of microprocessor architecture and high performance features in CISC architecture. This course familiarizes the high performance features in RISC architecture and introduces the basic features in Motorola microcontrollers and PIC Microcontroller

Microprocessor Architecture

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

32-BIT Microprocessors

Intel 80386 Microprocessor: Architecture - Registers – Descriptors - Real Mode - Protected mode - Virtual 8086 mode - Paging and Segmentation - Comparison with 80486 Microprocessor. Pentium class of processors: RISC and CISC architectures - Superscalar Architecture - MMX technology – SSE – Pipelining - Branch Prediction techniques – FPU - Comparative study of features of Pentium-II, Pentium-III and Pentium-IV processors.

64 -BIT Microprocessors

Intel 64 bit processors-:Overview of 64 bit processor execution environment – Memory organization – IA-32 memory models – Memory organization in 64 bit mode – Extended physical addressing in protected mode - Basic program execution registers – Operand addressing. Multicore Architectures: Concepts – Power reduction techniques in processors – Comparison of Intel Skylake,Goldmont and Ice Lake microarchitectures

High Performance Risc Architecture

Cortex-M Architecture: Introduction to Cortex-M Microcontroller, Microprocessor Architecture, Nested Interrupt Vector Controller, Bus System and Bus Matrix, Memory and Peripherals, Debug Systems, Exceptions and Interrupts Architecture, The ARM64 CPU Architecture, ARM CPU Registers The Memory Subsystem, ARM- 16/32 bit THUMB instruction set.

PIC Microcontrollers

The PIC32 : Pins, Peripherals, and Special Function Registers, PIC32 ,The Physical Memory Map, Virtual Memory Map, Configuration Bits, Interrupts, Digital I/O, Counter/Timers, I2C Interfacing –UART, SPI, Flash memory.

Activity:

Write a summary of architectural features of Microprocessors designed and developed in India such as VEGA Microprocessors.

References:

1. Breg, B. B. (2008). *The Intel microprocessors: Architecture, programming and interfacing*. PHI.
2. Tahir, M., & Javed, K. (2017). *ARM® microprocessor systems: Cortex®-M architecture, programming, and interfacing*. CRC Press.
3. Lynch, K. M., Marchuk, N., & Elwin, M. L. (2015). *Embedded computing and mechatronics with the PIC32 microcontroller*. Newnes, Elsevier.
4. Hyde, R. (2025). *The art of ARM assembly, Volume 1: 64-bit ARM machine organization and programming*. No Starch Press.
5. Tabak, D. (2011). *Advanced microprocessors* (2nd ed.). McGraw Hill.
6. Furber, S. (2014). *ARM system-on-chip architecture*. Addison Wesley.
7. Miller, G. H. (2003). *Micro computer engineering*. Pearson Education.
8. Intel. (n.d.). *Intel® 64 and IA-32 architectures software developer's manual: Vol. 1*. Intel Corporation. https://www.intel.com
9. MIT OpenCourseWare. (n.d.). *OpenCourseWare*. https://www.ocw.mit.edu
10. ARM. (n.d.). *ARM official website*. https://www.arm.com

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand microprocessor architecture, instruction sets, addressing modes, memory hierarchy, pipelining, and RISC vs CISC concepts	-	-	-
CO2	Analyze 32-bit Intel microprocessors (80386, Pentium series), superscalar architecture, MMX/SSE, branch prediction, and floating-point unit operations	PO3(3), PO4(3), PO5(2)	3	3
CO3	Understand 64-bit Intel processors, memory models, program execution registers, multicore architectures, and power reduction techniques	PO3(3), PO4(3), PO5(2)	3	3
CO4	Understand high-performance RISC architectures including ARM Cortex-M, ARM64, and PIC32 microcontrollers, along with memory, peripherals, interrupts, and interfacing protocols	PO3(3), PO4(3), PO5(2)	3	3

AP25003	Advanced Computer Architecture Design	L	T	P	C
		3	0	0	3

Course Objectives:

This course enables the students to understand the concepts of parallelism, partitioning and scheduling. It also deals with the hardware technologies and scalable architectures. It also enables the students to understand the Vector processing Principles and SIMD Computer Organisation.

Theory OF Parallelism

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

Partitioning and Scheduling

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance - performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

Hardware Technologies

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory – Bus Arbitration, cache memory organisations, shared memory organisations, sequential and weak consistency models.

Pipelining, Superscalar, Parallel and Scalable Architecture

Linear and Non-Linear Pipeline processor – Instruction and Arithmetic Pipeline Design – Superscalar and Superpipeline Design – Multiprocessor Interconnects – Cache Coherence and Synchronization mechanism – Message Passing Mechanism – Flow Control Strategies – Multicast Routing Strategies

Multivector and Simd Computers

Vector processing Principles – Compound Vector Processing – SIMD Computer Organisation – Synchronized MIMD machine – Latency Hiding Technique – Multithreading –Scalable and Multithreaded Architectures – Data Flow and Hybrid Architectures - Parallel models, Languages and compilers, Parallel program development and environments.

Activities:

1. Quiz for each unit.
2. Flipped classroom activity
3. Students will submit a report on recent commercial processors and their architectural aspects.

References:

1. Hwang, K. (2003). *Advanced computer architecture*. McGraw Hill International.
2. Sima, D., Fountain, T., & Kacsuk, P. (2003). *Advanced computer architecture: A design space approach*. Pearson Education.

3. Shen, J. P. (2003). *Modern processor design: Fundamentals of superscalar processors*. Tata McGraw Hill.
4. Hwang, K. (1998). *Scalable parallel computing*. Tata McGraw Hill.
5. Stallings, W. (2013). *Computer organization and architecture* (9th ed.). Macmillan Publishing Company.
6. Quinn, M. J. (1994). *Designing efficient algorithms for parallel computers*. McGraw Hill International.
7. Wilkinson, B., & Allen, M. (2005). *Parallel programming* (2nd ed.). Pearson Education Asia.
8. Jordan, H. F., & Alaghband, G. (2003). *Fundamentals of parallel processing*. Pearson Education.
9. Kain, R. Y. (2003). *Advanced computer architecture: A systems design approach*. PHI.
10. https://onlinecourses.nptel.ac.in/noc22_cs10/preview

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand the fundamentals of parallelism, computer models, PRAM and VLSI models, and conditions for parallel execution	-	-	-
CO2	Analyze program partitioning, scheduling, system interconnects, and performance scalability in parallel systems	PO2(3), PO3(3), PO4(2)	3	3
CO3	Understand hardware technologies including advanced processor designs, memory hierarchy, superscalar and vector processors, cache and shared memory organizations	PO3(3), PO4(3), PO5(2)	3	3
CO4	Understand pipelining, superscalar, SIMD, multivector, multithreaded and scalable architectures, synchronization, and parallel programming models	PO3(3), PO4(3), PO5(2)	3	3

AP25C05	Signal Integrity for High Speed Design	L	T	P	C
		3	0	0	3

Course Objective:

The objective of this course is to introduce students to the principles and challenges of maintaining signal integrity in high-speed digital designs. It aims to provide a comprehensive understanding of transmission line behavior, impedance control, reflections, crosstalk, differential signaling, and clock distribution. The course emphasizes practical analysis, modeling, and mitigation techniques used in designing robust and reliable high-speed digital systems.

Introduction

Introduction to Signal Integrity, Signal Quality on a Single Net, Cross Talk, Rail-Collapse Noise, Electromagnetic Interference (EMI), Signal-Integrity Solutions in Terms of Impedance: Impedance of ideal resistor, capacitor and inductor in time domain, Impedance in the Frequency Domain, Bulk Resistivity, Resistance per Length, Sheet Resistance, Power and Ground Planes and Decoupling Capacitance, Capacitance per Length, Self-Inductance and Mutual Inductance, Partial Inductance Effective, Total, or Net Inductance and Ground Bounce, Loop Self- and Mutual Inductance, Loop Inductance per Square of Planes, Loop Inductance of Planes and Via Contacts

Activity:

1. **Simulation Assignment:** Use EDA tools like LTspice to simulate impedance mismatch and analyze signal degradation on a PCB trace.
2. **Poster Presentation:** Students prepare a poster explaining impedance behavior in the time vs frequency domain, and the concept of ground bounce and EMI.

Transmission Lines and Reflections

Speed of a Signal in a Transmission Line, Instantaneous Impedance of a Transmission Line, Characteristic Impedance and Controlled Impedance, Return Paths , Frequency Variation of the Characteristic Impedance, Reflections, Reflections from Resistive Loads, Source Impedance, Bounce Diagrams, Reflections from Short Series andShort-Stub Transmission Lines, Reflections from Capacitive End Terminations, Reflections from Capacitive Loads in the Middle of a Trace, Capacitive Delay Adders, Effects of Corners and Vias, Loaded Lines, Reflections from Inductive Discontinuities, Compensation, Losses in Transmission Lines, Sources of Loss: Conductor Resistance and Skin Depth, The Dielectric, Dissipation Factor

Activity:

1. **Flipped Classroom:** Students review pre-recorded videos on reflection and impedance mismatch; classroom used for solving bounce diagram exercises.
2. **Hands-on Lab:**Build and measure signal reflection and delay using a coaxial cable, function generator, and oscilloscope (or simulation-based equivalent).

Crosstalk

Coupling: Capacitance and Inductance, Cross Talk in Transmission Lines, Cross Talk in Uniform Transmission Lines and Saturation Length, Capacitively Coupled Currents, Inductively Coupled Currents, Near-End Cross Talk, Far-End Cross Talk, Decreasing Far-End Cross Talk, Guard Traces, Cross Talk and Dielectric, Cross Talk and Timing, Switching Noise.

Activity:

1. **Case Study Analysis:**Analyze real PCB designs or documented failures where crosstalk affected system reliability (e.g., DDR memory buses, HDMI lines).
2. **Mini Quiz / Diagram Exercis**e: Conduct a quick in-class quiz identifying near-end and far-end crosstalk with diagram-based questions.

Differential Signaling

Differential Signaling, A Differential Pair, Differential Impedance with No Coupling, The Impact from Coupling, Calculating Differential Impedance, The Return-Current Distribution in a Differential Pair, Ideal Coupled Transmission-Line Model or an Ideal Differential Pair, Cross Talk in Differential Pairs, Crossing a Gap in the Return Path.

Activity:

1. **Simulation/Modeling Task:** Use EDA tools to model differential pairs and evaluate the effects of spacing and return path discontinuities.
2. **Group Presentation:** Students present on how differential signaling improves noise immunity and is used in USB, PCIe, or HDMI.

Clock Distribution and Clock Oscillators

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

Activity:

1. Timing Budgeting Exercise: Given a real-world high-speed system, students calculate skew, jitter, and timing margins for clock distribution.
2. Seminar / Tech Talk **:** Students present on advanced clocking techniques (e.g., PLLs, low-jitter buffers) and common clock distribution topologies.

References:

1. Bogatin, E. (Year). *Signal and power integrity simplified* (3rd ed.). Pearson.
2. Johnson, H., & Graham, M. (Year). *High speed digital design*. Prentice Hall.
3. Johnson, H. (Year). *High speed signal propagation*. Prentice Hall.

E-Resources

1. https://www.youtube.com/watch?v=YFwHV2EMB2A
2. https://suddendocs.samtec.com/notesandwhitepapers/samtec-signal-integrity-handbook.pdf
3. https://www.youtube.com/watch?v=KkfKQDnWf20
4. https://onlinecourses.nptel.ac.in/noc24_ee67/preview

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Understand the fundamental concepts of signal integrity and analyze the effects of impedance, capacitance, and inductance on signal quality in high- speed circuits.	-	-	-
CO2	Analyze transmission line behavior, identify causes of signal reflection, and apply impedance matching techniques to minimize reflections and losses.	PO3(3)	3	3
CO3	Examine the sources and effects of crosstalk in high-speed designs and propose methods to mitigate timing and noise-related issues.	PO1(3)	3	3
CO4	Understand and evaluate differential signaling concepts, including impedance calculation, coupling effects, and return current paths.	PO1(3) PO(2)	2	3

AP25004	VLSI Interconnects	L	T	P	C
		3	0	0	3

Course Objectives:

The objective of this course is to explore the concept of designing and modeling of VLSI interconnects and to study the effect of crosstalk noise and delay in electrical signal transmission through interconnects. This course also aims to introduce the techniques that can be adopted to mitigate the effect of crosstalk noise and delay in electrical signal transmission via VLSI interconnects. It further explores the the analysis of failures due to electromigration in VLSI Interconnection

Introduction

Types of interconnects, Interconnect Trends, Coupling capacitance, Inductive effects, Interconnect metrics, Signal transmission on interconnects, On-chip interconnections, Package level interconnections, Design Methodologies for Interconnect, Stress void and Electromigration phenomenon, Interconnections for VLSI Applications, Copper Interconnections, Fabrication and Damascene processing, Scaling of interconnects.

Interconnect Modeling

Lossless and Lossy transmission line model, Optimum line model selection, Circuit Models of Interconnect - Ideal, Capacitive, Resistive Interconnects, Resistive Interconnect Trees, Scaling Effects on Interconnect Delay, Cross-Capacitances and Their Decoupling with Miller Factor, Interconnect Power.

Crosstalk in Interconnects

Definition of Cross talk, Mutual inductance and mutual capacitance, Inductance and capacitance matrix, crosstalk-induced noise, simulating crosstalk using equivalent circuit models, Minimization of crosstalk, Crosstalk induced delay - Energy dissipation due to crosstalk- Crosstalk effects in logic VLSI circuits.

Noise Detection and Avoidance in Interconnects

Cross talk avoidance, Switching noise avoidance, noise detection problem, crosstalk-induced spurious signal detection, IDDx test approaches to crosstalk detection.

Electromigration-Induced Failure Analysis

Electromigration in VLSI Interconnection Metallizations, Modeling of Electromigration Due to Repetitive Pulsed Currents, Electromigration in Copper Interconnections, Failure Analysis of VLSI Interconnection Components, Computer-Aided Failure Analysis.

Future Interconnections

Demands in Future Interconnects, Introduction to optical and superconducting interconnects, Silicon Nano-wires and Metallic Interconnections, Nano-tube Interconnections, Quantum-Cell-Based Wireless Interconnections.

Activities:

- Design and simulate any two Circuit Models of Interconnect and observe their delay and power using EDA tools.
- Simulate crosstalk using equivalent circuit models using EDA tools.

- Read a recent research article on Future Interconnects and summarize the same and submit as a report.

References:

1. Goel, A. K. (2007). *High-speed VLSI interconnections* (2nd ed.). IEEE-Wiley.
2. Moll, F., & Roca, M. (2004). *Interconnection noise in VLSI circuits*. Kluwer Academic Publishers.
3. Celik, M., Pileggi, L., & Odabasioglu, A. (2002). *IC interconnect analysis*. Kluwer Academic Publishers.
4. Moiseev, K., Kolodny, A., & Wimer, S. (2015). *Multi-net optimization of VLSI interconnect*. Springer.
5. Hall, S. H., Hall, G. W., & McCall, J. A. (2000). *High-speed digital system design: A handbook of interconnect theory and design practices*. Wiley.
6. Saini, S. (2015). *Low power interconnect design*. Springer.
7. Kaushik, B. K., & Majumder, M. K. (2015). *Carbon nanotube based VLSI interconnects: Analysis and design*. Springer.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand the fundamentals of VLSI interconnects, types, scaling trends, and fabrication methods	-	-	-
CO2	Model interconnects using lossless/lossy transmission line models, circuit models, and analyze delay and power effects	PO3(3), PO4(3), PO5(2)	3	3
CO3	Analyze crosstalk noise, mutual coupling, and switching noise in interconnects and study techniques for minimization	PO3(3), PO4(3), PO5(2)	3	3
CO4	Understand electromigration-induced failures, advanced interconnect technologies (optical, nano-wire, quantum) and future trends	PO3(3), PO4(3), PO5(2)	3	3

AP25005	Semiconductor Memory Design	L	T	P	C
		3	0	0	3

Course Objective:

The objective of this course is to provide a comprehensive understanding of semiconductor memory technologies, their architecture, operation, testing methodologies, reliability considerations, and packaging techniques. It aims to enable students to analyze and evaluate the design and functionality of various memory types, including volatile, non-volatile, and advanced memory systems used in modern electronic devices and systems.

Random Access Memory Technologies

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation - Silicon on Insulator (SOI) Technology- SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-SoftError Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Activity:

1. **Simulation Lab:** Simulate SRAM and DRAM cell structures using LTspice or Cadence; analyze read/write cycles and power consumption.
2. **Poster Presentation:** Design posters comparing SRAM vs DRAM architectures, technologies, and applications (e.g., cache vs main memory).

Nonvolatile Memories

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

Activity:

1. **Seminar / Presentation:** Students give short talks on Flash, EEPROM, OTP, or EPROM structures and their role in real-world embedded systems.
2. **Flipped Classroom:** Assign students to study Flash memory architecture beforehand and solve design trade-off problems during class.

Memory Fault Modeling, Testing

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

Activity:

1. **Quiz / Fault Identification Task:** Conduct a quiz or task where students identify and classify memory fault types and appropriate test methods.
2. **Testing Demo / Lab Assignment:** Test RAM or EEPROM on microcontroller kits (Arduino/8051) using write-read verification codes.

Reliability and Radiation Effects

General Reliability Issues-RAM Failure Modes and Mechanism-Design for Reliability-Reliability Test Structures-Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics.

Activity:

1. **Case Study Presentation**: Analyze real-world memory failures due to soft errors or radiation (e.g., aerospace) and present mitigation methods.
2. **Poster / Report on Radiation Hardening**: Prepare a technical poster/report on radiation effects and hardening techniques used in memory design.

Advance D Memories and Packaging Technologies

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide(GaAs)FRAMs-Analog Memories-Magnetoresistive. Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues- Memory Cards-High Density Memory Packaging Future Directions.

Activity:

1. **Mini Project:** Design a conceptual hybrid memory module (e.g., MRAM + Flash) or stacked memory using 2D/3D MCM principles.
2. **Model Making / CAD Visualization:** Build physical or software models of memory stacks or advanced memory cell structures using tools like TinkerCAD or Fusion360.

References:

1. Sharma, A. K. (1997). *Semiconductor memories: Technology, testing and reliability*. Prentice-Hall of India Private Limited.
2. Haraszti, T. P. (2001). *CMOS memory circuits*. Kluwer Academic Publishers.
3. Prince, B. (2002). *Emerging memories: Technologies and trends*. Kluwer Academic Publishers.

E-Resources

1. https://archive.nptel.ac.in/courses/117/101/117101058/
2. https://onlinecourses.nptel.ac.in/noc21_cs47/preview?
3. https://archive.nptel.ac.in/courses/113/105/113105099/

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand the architecture, operation, and technologies of volatile memories (SRAM, DRAM)	-	-	-
CO2	Analyze nonvolatile memories (ROM, PROM, EPROM, EEPROM, Flash) and compare architectures	PO1(3), PO2(3), PO5(2)	3	2
CO3	Apply memory fault modeling, testing, and verification techniques for RAMs and nonvolatile memories	PO3(3), PO4(3), PO5(2)	3	3
CO4	Evaluate reliability, radiation effects, and advanced memory technologies including packaging and hybrid memories	PO3(3), PO4(3), PO5(2)	3	3

AP25006	Algorithms For VLSI Physical Design Automation	L	T	P	C
		3	0	0	3

Course Objectives:

The objective of this course is to understand the fundamentals of VLSI physical design cycle. It also introduces algorithms employed in each stage of VLSI physical design automation.

Introduction

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles –Review of VLSI Design Automation Tools.

Data Structures and Basic Algorithms

Basic Data Structures, Graph Algorithms: Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Classes of Graphs in Physical Design, Relationship Between Graph Classes, Graph Problems in Physical Design, Algorithms for Interval Graphs, Algorithms for Permutation Graphs, Algorithms for Circle Graphs

Algorithms for Layout Compaction, Placement and Partitioning

Layout Compaction: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint Graph Compaction – Placement and Partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithms, Partitioning: The Kernighan-Lin Partitioning Algorithm

Algorithms for Floorplanning and routing

Floorplanning: Floorplanning Concepts, Terminology and Floorplan Representation, Optimization Problems in Floorplanning, Shape Functions and Floorplan Sizing. Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing.

Modelling and Simulation and Synthesis

Simulation: Gate Level Modeling and Simulation, Switch-level Modeling and Simulation – Logic Synthesis and Verification: Combinational Logic Synthesis, Binary Decision Diagrams, Two-level Logic Synthesis, High level Synthesis.

Activities:

1. Simulate the complete VLSI physical design cycle for a simple circuit using suitable CAD tools.
2. Demonstrate Binary Decision Diagram for a chosen logic function with hand calculation.
3. Demonstrate various types of delay modeling at gate level with HDL

References:

1. Sherwani, N. A. (2017). *Algorithms for VLSI physical design automation* (3rd ed.). Springer.
2. Gerez, S. H. (2017). *Algorithms for VLSI design automation* (2nd ed.). Wiley-India.
3. Alpert, C. J., Mehta, D. P., & Sapatnekar, S. S. (n.d.). *Handbook of algorithms for physical design automation* (1st ed.). CRC Press.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand VLSI design methodologies, physical design cycle, and data structures used in CAD tools	-	-	-
CO2	Apply graph algorithms, layout compaction, placement, and partitioning techniques	PO3(3), PO4(3), PO5(2)	3	3
CO3	Analyze floorplanning and routing algorithms for VLSI physical design	PO3(3), PO4(3), PO5(2)	3	3
CO4	Implement modeling, simulation, and synthesis for VLSI designs using gate-level, switch-level, and combinational logic	PO3(3), PO4(3), PO5(2)	3	3

AP25007	Statistical Analysis and Optimization for VLSI	L	T	P	C
		3	0	0	3

Course Objectives:

- The objective of this course is to explore various sources of variation in VLSI design and to familiarize the students with the statistical models and techniques used in VLSI design. This course also aims to explore the methods of statistical timing power and yield analysis and optimization techniques for VLSI design

Introduction

Sources of Variations: Process, Environmental, Modeling and other Sources of Variations, Components of Variation: Inter-die Variations, Intra-die variations, Impact on Performance

Statistical Models and Techniques

Monte Carlo Techniques: Sampling Probability Distributions using Acceptance-Rejection Method and Multivariate Gaussian random variables, Process Variation Modeling: Pelgrom's Model, Principal Components Based Modeling, Quad-Tree Based Modeling, Electromigration Modeling, Performance Modeling: Response Surface Methodology, Delay Modeling, Interconnect Delay Models: Statistical Delay Metrics.

Statistical Timing Analysis

Introduction, Block-Based Timing Analysis, Discretized Delay PDFs, Reconvergent Fanouts, Canonical Delay PDFs, Multiple Input Switching, Path-Based Timing Analysis, Parameter-Space Techniques, Bayesian Networks

Statistical Power and Yield Analysis

Power Analysis: Leakage Models, High-Level Statistical Analysis, Gate-Level Statistical Analysis, Dynamic Power, Leakage Power: Estimating Parameters of the Distribution, Estimating the probability density function, Temperature and Power Supply Variations, Yield Analysis: High-Level Yield Estimation, Gate-Level Yield Estimation: Timing Analysis, Leakage Power Analysis, Yield Estimation, Supply Voltage Sensitivity

Statistical Optimization Techniques

Optimization of Process Parameters, Gate Sizing, Buffer Insertion, Threshold Voltage Assignment

Activities:

1. Perform process, voltage and temperature variation analysis using Monte-Carlo method and plot the probability density function for each parameter. (Use appropriate EDA tool)
2. Apply Bayesian Network for timing analysis for any benchmark circuit and estimate delay with hand calculations..

References

1. Srivastava, A., Sylvester, D., & Blaauw, D. (2005). Statistical analysis and optimization for VLSI: Timing and power. Springer.
2. Shen, R., Tan, S. X.-D., & Yu, H. (2012). Statistical performance analysis and modeling techniques for nanometer VLSI designs. Springer.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand sources of variation in VLSI designs and their impact on performance	-	-	-
CO2	Apply statistical models and Monte Carlo techniques for variation and performance analysis	PO3(3), PO4(3), PO5(2)	3	3
CO3	Perform statistical timing, power, and yield analysis using block-based and path-based methods	PO3(3), PO4(3), PO5(2)	3	3
CO4	Optimize VLSI circuits using gate sizing, buffer insertion, and threshold voltage assignment	PO3(3), PO4(3), PO5(2)	3	3

AP25008	System-On-Chip (SOC) Design	L	T	P	C
		3	0	0	3

Course Objective:

This course introduces the architecture, design methodologies, and customization techniques involved in developing Systems-on-Chip (SoCs). The emphasis is on embedded processor selection, memory design, interconnects, and FPGA-based implementations. Students will learn to optimize area, power, and performance for advanced electronic applications.

System Architecture: Overview

Components of the system – Processor architectures – Memory and addressing – System-level interconnection – SoC design requirements and specifications – Design integration – Design complexity – Cycle time, die area and cost – Ideal and practical scaling – Area-time-power tradeoff in processor design – Configurability.

Activity: Seminar, Quiz, Flipped classroom

Processor Selection for SOC

Overview – Soft processors, processor core selection – Instruction set, branches, interrupts and exceptions – Basic elements in instruction handling – Minimizing pipeline delays – Reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

Activity: Seminar, Quiz, Flipped classroom

Memory Design

SoC external memory, SoC internal memory – Scratchpads and cache memory – Cache organization and write policies – Line replacement strategies – Split I/D-caches – Multilevel caches – SoC memory systems – Board-based memory systems – Processor/memory interaction.

Activity: Collaborative Learning

Interconnect Architectures and SOC Customization

Bus architectures – SoC standard buses (AMBA, Core Connect) – Processor customization approaches – Reconfigurable technologies – Mapping designs onto reconfigurable devices – FPGA-based design – Architecture of FPGA – FPGA interconnect technology – FPGA memory – Floor planning and routing

Activity: Project-Based Learning

FPGA-Based Embedded Processor

Hardware/software task partitioning – FPGA fabric-immersed processors – Soft processors and hard processors – Tool flow for hardware/software co-design – Interfacing processor with memory and peripherals – On-chip interfaces: Wishbone, Avalon, OPB – Customized microcontroller design – FPGA-based signal interfacing and conditioning.

Activity: Industry / Field Visits.

References

1. Flynn, M. J., & Luk, W. (2011). Computer system design: System-on-chip. Wiley India.
2. Furber, S. (2000). ARM system-on-chip architecture (2nd ed.). Addison-Wesley.
3. Vahid, F. (2001). Embedded system design: A unified hardware/software introduction. Wiley.
4. Patterson, D. A., & Hennessy, J. L. (2013). Computer organization and design: The hardware/software interface (5th ed.). Morgan Kaufmann.
5. Lin, Y.-L. S. (Ed.). (2007). Essential issues in SoC design. Springer.
6. Elmasry, M. I. (2002). System-on-chip for real-time applications. Springer.
7. Kamal, R. (2020). Embedded systems: Architecture, programming and design (3rd ed.). McGraw Hill.
8. Kaeslin, H. (2008). Digital integrated circuit design: From VLSI architectures to CMOS fabrication. Cambridge University Press.
9. Wolf, W. (2009). Modern VLSI design: IP-based design (4th ed.). Pearson Education.

E-Learning Resources:

1. NPTEL Course on "System on Chip Design" by Prof. S. Kamakoti, IIT Madras – https://nptel.ac.in
2. Coursera – *SoC Design Lab* and *FPGA-based Embedded Systems* by University of Colorado Boulder
3. edX – *Computer Architecture and Design* by MITx
4. ARM Developer Resources – https://developer.arm.com
5. Xilinx/Vivado Tutorials and Docs – https://www.xilinx.com
6. Intel FPGA Training – https://www.intel.com/fpga

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand SoC system architecture, components, interconnects, and trade-offs in area, power, and performance	-	-	-
CO2	Analyze and select appropriate processors for SoC including soft, hard, VLIW, and superscalar processors	PO3(3), PO4(2)	3	3
CO3	Design and organize SoC memory systems including caches, scratchpads, and multi-level memory hierarchies	PO3(3), PO4(3)	3	3
CO4	Implement SoC designs on FPGAs, customize processors, map designs, and manage hardware/software partitioning	PO3(3), PO4(3), PO5(2)	3	3
CO5	Interface embedded processors with peripherals and standard on-chip communication protocols (Wishbone, Avalon, OPB)	PO3(3), PO4(3)	3	3

AP25C06	Hardware / Software Co-Design	L	T	P	C
		3	0	0	3

Course Objectives:

The objective of this course is to acquire the knowledge about system specification and modeling and to learn the formulation of partitioning. This course also deals with the different technical aspects about prototyping, emulation and verification.

System Specification and Modelling

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification And Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures With One ASIC, Single-Processor Architectures With Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification.

Hardware/Software Partitioning

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

Hardware/Software Co-Synthesis

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis – Hardware/software co-synthesis algorithms: hardware – software partitioning, distributed system co-synthesis.

Prototyping and Emulation

Introduction, Prototyping And Emulation Techniques, Prototyping and Emulation Environments, Future Developments In Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

Design Specification and Verification

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design: System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation

References:

1. Schaumont, P. (2010). A practical introduction to hardware/software codesign. Springer.
2. Niemann, R. (1998). Hardware/software co-design for data flow dominated embedded systems. Kluwer Academic Publishers.
3. Staunstrup, J., & Wolf, W. (1997). Hardware/software co-design: Principles and practice. Kluwer Academic Publishers.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%
Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Describe the broad range of system architectures and design methodologies that currently exist and define their fundamental attributes.	-	-	-
CO2	Apply the dataflow models as a state-of-the-art methodology to solve co-design problems and to optimize the balance between software and hardware	PO3(3)	2	3
CO3	Develop co-design solutions to problems using modern hardware/software tools for building prototypes.	PO1(3)	3	2
CO4	Identify the concurrent specification from an algorithm, analyze its behavior and partition the specification into software and hardware components	PO1(3) PO(2)	2	3

VL25C02	MEMS & NEMS	L	T	P	C
		3	0	0	3

Course Objective:

- To understand MEMS fundamentals and fabrication processes.
- To impart knowledge of the photolithographic process, photo resist and pattern transfer.
- To provide a fundamental of NEMS and its fabrication methods.
- To explore carbon-based NEMS materials and fabrication challenges.
- To learn about the diverse applications of MEMS and NEMS.

Fundamentals of MEMS

MEMS Introduction - Low Cost - Redundancy and Disposability – Scaling – Made – Substrates –Processing – Mask – Developing – Etching - Road Map and Perspective Silicon Substrate – Silicon Growth – Crystal - Miller Indices – Semiconductor – Doping - Additive Techniques.

Activity:

- **Case Study**: Analyze the evolution and cost benefits of MEMS in healthcare diagnostics.
- **Hands-on**: Silicon wafer orientation and doping simulation using open tools (e.g., NanoHUB).

Pattern Transformation of Mems

Photolithographic Process - Clean room - Photo Resist - Positive Resist - Negative Resist –Working with Resist – Applying Photo Resist - Exposure and Pattern Transfer - Printing Methods – Contact Proximity – Projection Printing - Development and Post Treatment -Masks – Resolution –Sensitivity and Resist Profiles – Mask Alignment - Permanent Resists

Activity:

- Lab Demo / Video Simulation: Lithography and mask alignment procedure
- Assignment: Design a basic mask layout for a MEMS pattern

Introduction of NEMS

Introduction – Basic properties - Benefits of Nanomachines – Miniaturization - NEMS Memory – Importance of AFM - Top-Down Approach - NEMS devices - NEMS Advantages.

Activity:

- Seminar: Benefits and miniaturization challenges in NEMS
- Simulation: NEMS memory modeling using nano-electronics simulator (NanoHub toolkit)

Feedback Amplifiers and Waveform Generators

Materials – Carbon Allotropes - Carbon Based Materials - Metallic Carbon Nanotubes – Difficulties – Simulations - Current Challenges and future of NEMS – Deposition processes – Lithography – Etching processes.

Activity:

- Group Project: Design and simulate a carbon nanotube-based NEMS device
- Quiz: On lithography types and carbon-based nanomaterials

Power Amplifiers Pressure sensor - Piezoresistive sensor - Capacitive sensor – RF applications – Gyroscope – Optical MEMS - Optical Data - Switching - RF MEMS - MEMS switches - MEMS Resonators. Case study: Cantilever piezoelectric actuator, Capacitive accelerometer, Piezoresistive pressure sensor **Activity:** • Case Study Presentation: Comparison of MEMS gyroscope and accelerometer • Assignment: Technical report on emerging RF MEMS switches.
Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%
Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Explain the fundamentals of MEMS including materials, silicon substrates, fabrication processes, scaling concepts, and applications in sensing and actuation.	-	-	-
CO2	apply photolithographic and pattern transfer processes for MEMS device fabrication, including mask design and resist processing.	PO3(3)	3	2
CO3	Analyze the principles, materials, fabrication challenges, and performance of NEMS devices including carbon-based nanomaterials and feedback-based nanodevices.	PO1(3)	3	2
CO4	Design and evaluate MEMS/NEMS-based sensors, actuators, and RF/optical MEMS devices using simulations and case studies.	PO1(3) PO(2)	2	3

EL25C01	Cryptography and Network Security	L	T	P	C
		3	0	0	3

Course Objectives:

This course aims to provide an understanding of the importance and objectives of communication network and information security, along with an overview of various types of attacks. It introduces different security approaches and algorithms used to ensure data integrity and authenticity. The course also emphasizes the practical design and implementation of security features in both wired and wireless networking environments.

Introduction on Security: Security Goals, Cryptographic attacks, Security services and

mechanisms Techniques: Cryptography and Steganography, Traditional Symmetric-Key Ciphers: Substitution Ciphers and Transposition Ciphers, Mathematics for Cryptography.

Symmetric & Asymmetric Key Algorithms: Introduction to Block Ciphers and Stream Ciphers, Data Encryption Standards (DES), Advanced Encryption Standard (AES), RC4, Principle of asymmetric key algorithms, RSA Cryptosystem.

Integrity, Authentication and Key Management: Message Integrity, Hash functions: SHA 512, Whirlpool, Digital signatures: Digital signature standards. Authentication: Entity Authentication: Biometrics, Key management Techniques.

Network Security, Firewalls and Web Security: Introduction on Firewalls, Types of Firewalls, IP Security, E-mail security: PGP- S/MIME, Web security: SSL-TLS, SET.

Wireless Network Security: Security Attack issues specific to Wireless systems: Worm hole, Tunneling, DoS. Security for WLAN, Security for Broadband networks: Security challenges in 4G and 5G deployments, Introduction to side channel attacks and their counter measures.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

References

1. Behrouz A. Forouzan ,"Cryptography and Network security", McGraw- Hill, 2011
2. William Stallings, "Cryptography and Network security: principles and practice", Prentice Hall of India, New Delhi, 2nd Edition,2002
3. AtulKahate ,"Cryptography and Network security", Tata McGraw-Hill,2nd Edition, 2008.
4. R.K.Nichols and P.C. Lekkas ,"Wireless Security: Models , threats and Solutions", McGraw- Hill, 2001.
5. H. Yang et al., "Security in Mobile Ad Hoc Networks: Challenges and Solution", IEEE Wireless Communications, Feb. 2004.
6. "Securing Ad Hoc Networks", IEEE Network Magazine, vol. 13, no. 6, pp. 24-30, December 1999.

7. "Security of Wireless Ad Hoc Networks," http://www.cs.umd.edu/~aram/wireless/survey.pdf
8. David Boelet.al,“Securing Wireless Sensor Networks – Security Architecture”, Journal of networks , Vol.3. No. 1. pp. 65 -76, Jan 2008.
9. Perrig, A., Stankovic, J., Wagner, D., “Security in Wireless Sensor Networks”, Communications of the ACM, 47(6), 53-57, 2004.

. Introduction to side channel attacks – http://gauss.ececs.uc.edu/Courses/c653/lectures/SideC/intro.pdf.

	CO description	PO Mapping	PSO1	PSO2
CO1	Explain security goals, cryptographic attacks, security services, mechanisms, and classical cryptographic techniques including symmetric-key ciphers and cryptographic mathematics.	-	-	-
CO2	Apply symmetric and asymmetric key algorithms such as DES, AES, RC4, and RSA with respect to confidentiality and performance.	PO1(3)	3	3
CO3	Evaluate integrity, authentication, hashing algorithms, digital signature schemes, and key management techniques for secure communication.	PO23)	3	3
CO4	Analyze and design security mechanisms for network, web, and wireless systems including firewalls, IPsec, SSL/TLS, WLAN security, and 4G/5G security challenges.	PO3(3) PO4(2)	2	3

AP25009	Neuromorphic Computing	L	T	P	C
		3	0	0	3

Course Objectives:

This course introduces the biological foundations of neural computation and synaptic plasticity. Students will analyse spiking neural networks and design CMOS/VLSI circuits for neuromorphic systems. It also covers hardware architectures like Loihi and SpiNNaker, with a focus on low-power applications in sensing and robotics.

Biological Inspiration and Neural Coding

Biological neurons and synapses: structure and function, Spike generation and propagation (Hodgkin-Huxley, Integrate-and-Fire models), Neural coding: rate code, temporal code, population code, Synaptic plasticity: Hebbian learning, STDP (Spike-Timing-Dependent Plasticity), Functional models of neural computation

Activity: Simulating Neural Spiking and Coding

Spiking Neural Networks and Learning Algorithms

SNN architecture and neuron models (LIF, Izhikevich), Spike encoding and decoding techniques, Supervised and unsupervised learning: STDP, Reward-Modulated STDP, Reservoir computing and Liquid State Machines, SNN simulation frameworks: BRIAN2, NEST, PyNN.

Activity: Build and Train a Simple Spiking Neural Network Using BRIAN2

VLSI Implementation of Neuromorphic Systems

Analog and digital circuit models of neurons and synapses, Current-mode vs. voltage-mode designs, Subthreshold analog VLSI design for neuron circuits, Mixed-signal implementations and silicon neurons, Noise tolerance and power-efficiency in neuromorphic chips

Activity: Design and Simulate a Subthreshold Analog Silicon Neuron

Neuromorphic Hardware and Architectures

Architectures of Loihi (Intel), TrueNorth (IBM), SpiNNaker (Manchester), Memory-centric computing and synapse mapping, Memristor-based neuromorphic architectures, Emerging devices: Phase-change memory, Ferroelectric FETs, and STT-MRAM, Crossbar arrays and 3D integrated neuromorphic systems

Activity: Compare and Analyze Modern Neuromorphic Hardware Architectures

Applications and Trends in Neuromorphic Computing

Brain-computer interfaces (BCI), Edge computing using neuromorphic chips, Sensor fusion and neuromorphic perception (vision, auditory), Neuromorphic robotics and event-based control, Future directions: AI accelerators, quantum neuromorphic systems, ethical implications.

Activity: Design a Neuromorphic Application for Edge Intelligence

References

1. Gerstner, W., Kistler, W. M., Naud, R., & Paninski, L. (2014). Neuronal dynamics: From single neurons to networks and models of cognition. Cambridge University Press.
2. Chen, Y., Chen, T., & Li, L. (2023). Neuromorphic computing systems: Architectures, models and applications. Springer.
3. Mead, C. (1989). Analog VLSI and neural systems. Addison-Wesley.
4. Koch, C. (2004). Biophysics of computation: Information processing in single neurons. Oxford University Press.
5. Furber, S. (2006). Principles of asynchronous circuit design: A systems perspective. Springer.

E-Resources

1. Neuronal Dynamics by Gerstner et al. http://neuronaldynamics.epfl.ch/
2. MIT OCW – Principles of Neuroscience https://ocw.mit.edu/courses/brain-and-cognitive-sciences/9-01-introduction-to-neuroscience-fall-2007/

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand types of VLSI interconnects, scaling trends, and copper/interconnect fabrication	-	-	-
CO2	Model interconnects using lossy/lossless transmission line models and analyze delay/power	PO3(3), PO4(2), PO5(2)	3	2
CO3	Analyze crosstalk and switching noise, and apply techniques for noise detection and avoidance	PO3(3), PO4(3)	3	2
CO4	Understand electromigration failures and explore emerging interconnect technologies	PO3(3), PO4(2), PO5(2)	3	2

AP25010	Artificial Intelligence Hardware Design	L	T	P	C
		3	0	0	3

Course Objectives:

The objective of this course is to learn the design aspects of artificial intelligence hardware. This course explores various parallel architectures and computation methods for efficient artificial intelligence hardware implementation

Introduction to Deep Learning

Development History, Neural Network Models, Neural Network Classification, Neural Network Framework, Neural Network Comparison, Neural Network Layers, DNN Development Resources, Deep Learning Challenges, Key Metrics and Design Objectives.

Parallel Architectures

Central Processing Unit (CPU), Graphics Processing Unit (GPU), Deep Learning Accelerator (NVDLA), Tensor Processing Unit (TPU), Catapult Fabric Accelerator. Streaming Graph Theory: Blaize Graph Streaming Processor Graphcore Intelligence Processing Unit

Convolution Optimization

Deep Convolutional Neural Network Accelerator, Eyeriss Accelerator

In-Memory Computation and Near-Memory Architecture

Neurocube Architecture, Tetris Accelerator, NeuroStream Accelerator, DaDianNao Supercomputer, Cnvlutin Accelerator

Network Sparsity

Energy Efficient Inference Engine, Cambricon-X Accelerator, SCNN Accelerator, SeerNet Accelerator

3D Neural Processing

3D Integrated Circuit Architecture, Power Distribution Network, 3D Network Bridge, Power- Saving Techniques

Activities:

1. Sketch the architecture of well known DNN and analyze the parameters and number of computations in each layer.
2. Compare and contrast the key features of various parallel architectures and write a report on the same. Consider a real time problem, and identify which architecture will be suitable for that problem. Justify your answer.
3. Analyze the effect of filter size on the performance of DNN.
4. Read a recent research article on hardware implementation strategies of Artificial Intelligence algorithms and summarize the same and submit as a report.

References:

1. Liu, A. C. C., & Law, O. M. K. (2021). Artificial intelligence hardware design: Challenges and solutions. IEEE–Wiley.
2. Sze, V., Chen, Y.-H., Yang, T.-J., & Emer, J. S. (2020). Efficient processing of deep neural networks. Morgan & Claypool.
3. Goodfellow, I., Bengio, Y., & Courville, A. (2016). Deep learning. MIT Press. https://www.deeplearningbook.org
4. Thakare, A. D., & Bhandari, S. U. (2023). Artificial intelligence applications and reconfigurable architectures. Wiley & Scrivener.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand deep learning models, layers, frameworks, and design objectives for AI hardware	-	-	-
CO2	Analyze and compare parallel architectures (CPU, GPU, TPU, NVDLA, IPU) for AI hardware	PO3(3), PO5(2), PO4(2)	3	2
CO3	Explore optimization techniques for convolutional neural network accelerators	PO3(3), PO4(2)	3	2
CO4	Study emerging AI hardware designs: in-memory computation, 3D integration, energy-efficient architectures	PO3(3), PO4(3), PO5(2)	3	2

AP25011	IP Core Design and Protection	L	T	P	C
		3	0	0	3

Course Objectives:

- The objective of this course is to introduce IP core design concepts and to explore the strategies for hardware IP protection and IP authentication methods.

IP Cores Design

Introduction: IP cores in a typical VLSI design flow, Classification of hardware IP, IP Modeling, IP Verification, IP Optimization, IP Protection, Gates as IP, Subsystems as IP, IP Components, Intellectual Property in Reuse-Based Design

Hardware Intellectual Property Protection

Functional Obfuscation through State Transition Graph Modification, Extension of STG Modification for RTL Designs, Obfuscation through Control and Dataflow Graph (CDFG) Modification, Measure of Obfuscation Level, Design Flow, Implementation Results, Effect of Key Length

Constraint-Based IP Protection

Solutions to SAT, FPGA Design of DES Benchmark, Graph Coloring and the CF IIR Filter Design, Constraint-Based Watermarking, Fingerprinting, Copy Detection, Challenges and the Generic Approach, Mathematical Foundations for the Constraint-Based Watermarking Techniques, Optimization-Intensive Watermarking Techniques.

IP User's Right Protection

Motivation and Challenges, Fingerprinting Objectives, Constraint-Based Fingerprinting Techniques

IP Authentication

Introduction, Pattern Matching Based Techniques, Forensic Engineering Techniques, Public Detectable Watermarking Techniques.

Activities:

- Quiz for each module.
- Write a report on Watermarking Techniques used in IP protection and authentication.
- Analyze the effect of key length on hardware IP protection.

References:

1. Wolf, W. (2009). Modern VLSI design: IP-based design. Pearson Education.
2. Mohamed, K. S. (2016). IP cores design: From specifications to production. Springer.
3. Mukhopadhyay, D., & Chakraborty, R. S. (2015). Hardware security: Design, threats, and safeguards. CRC Press.
4. Qu, G., & Potkonjak, M. (2003). Intellectual property protection in VLSI designs: Theory and practice. Kluwer Academic Publishers.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand IP core concepts, classification, modeling, verification, and optimization	-	-	-
CO2	Explore functional obfuscation and hardware IP protection techniques	PO3(3), PO4(2), PO5(2)	3	2
CO3	Study constraint-based IP protection techniques including watermarking, fingerprinting, and copy detection	PO3(3), PO4(2)	3	2
CO4	Analyze IP authentication methods using pattern matching and forensic engineering	PO3(3), PO4(3), PO5(2)	3	2

AP25012	Spintronics and Quantum Computing	L	T	P	C
		3	0	0	3

Course Objectives:

This course covers the fundamentals of spin dynamics and spintronic effects in modern electronic materials. It examines the operation of spin-based devices and introduces essential quantum computing concepts such as qubits, gates, and algorithms. Students will also analyze hardware implementations and explore the integration of spintronics with quantum computing platforms.

Fundamentals of Spintronics

Electron spin, spin angular momentum, Pauli exclusion principle, Ferromagnetism, magnetic domains, exchange interaction, Spin injection and detection, Giant magnetoresistance (GMR), tunneling magneto resistance (TMR), Spin polarization and spin coherence.

Spin-Based Devices and Architectures

Spin valves, magnetic tunnel junctions (MTJs), Spin Field Effect Transistors (SpinFETs), Domain wall logic and racetrack memory, Spin torque oscillators, STT-MRAM, SOT devices, Fabrication challenges and materials for spintronic devices

Introduction to Quantum Computing

Qubits: physical realization and quantum state representation, Quantum gates and circuits: single- and multi-qubit operations, Quantum superposition and entanglement, No-cloning theorem and quantum teleportation, Reversible logic and quantum circuit metrics

Quantum Algorithms and Error Correction

Quantum parallelism and the Deutsch-Jozsa algorithm, Grover's algorithm and search speedup, Shor's algorithm for integer factorization, Quantum error correction codes (bit flip, phase flip, Shor code), Basics of quantum fault tolerance

Hardware Realizations and Spin-Qubit Integration

Physical qubit implementations: superconducting, trapped ion, spin qubits; Semiconductor spin qubits: GaAs and Si-based platforms, NV centers in diamond and quantum dots, Integration of spintronics with quantum computing hardware, Cryogenic control and coherence time limitations.

References

1. Bandyopadhyay, S., & Cahay, M. (2015). Introduction to spintronics (2nd ed.). CRC Press.
2. Awschalom, D. D., Loss, D., & Samarth, N. (2002). Semiconductor spintronics and quantum computation. Springer.
3. Nielsen, M. A., & Chuang, I. L. (2010). Quantum computation and quantum information. Cambridge University Press.
4. Hofmann, P. (2015). Solid state physics: An introduction. Wiley-VCH.
5. Tucci, R. R. (2022). Qiskit textbook: Learn quantum computing using Qiskit (Online ed.). IBM Quantum/Open Source.

E-Resources

1. NPTEL Course: Spintronics – Physics and Technology by Dr. A. Perumal, IIT Guwahati
   https://nptel.ac.in/courses/115103039
2. Simulator: IBM Quantum Lab (Qiskit online simulator)
   https://learning.quantum.ibm.com/
3. MOOC Course: Quantum Computation (MITx)
   https://ocw.mit.edu/courses/6-845-quantum-complexity-theory-fall-2010/
4. Simulation/Tool: QuTiP Quantum toolbox in Python
   http://qutip.org

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%

Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

CO	CO Description	PO Mapping	PSO1	PSO2
CO1	Understand fundamental spintronics concepts: electron spin, magnetic domains, GMR/TMR, spin coherence	-	-	-
CO2	Analyze spin-based devices and architectures including MTJs, SpinFETs, STT-MRAM, racetrack memory	PO3(3), PO4(2)	3	2
CO3	Comprehend quantum computing principles: qubits, gates, superposition, entanglement, and circuits	PO1(3), PO2(3), PO4(2)	3	2
CO4	Study quantum algorithms, error correction techniques, and fault-tolerant computing	PO2(3), PO4(3), PO5(2)	3	2
CO5	Explore hardware implementations and integration of spintronics with quantum computing platforms	PO3(3), PO5(3)	3	3

CU25C14	Analog and Mixed Signal VLSI Design	L	T	P	C
		3	0	0	3

Course Objectives:

- To understand the fundamentals of Analog IC design, MOSFET models, and device-level noise behavior.
- To analyze and design CMOS analog building blocks including amplifiers, current mirrors, references, and op-amps.
- To explore mixed-signal design concepts and implement circuits like data converters, comparators, and PLLs.

Introduction

Introduction to Analog IC Design, Design Flow of Analog ICs, MOSFET Characteristics and Parameters, MOSFET Models, MOS Diode, MOS Capacitors, MOS Switches, Noise in MOSFETs.

CMOS Amplifiers

Single stage amplifiers: CS, CG and CD stages, Small Signal Models, Input Output Impedances, and Frequency Response. Differential Amplifier, Cascode Amplifiers, Current Amplifiers.

CMOS Sub-Circuits

Current Sinks and Sources, Simple and Cascode current Mirrors, Wilson Current Mirror, and High Swing Current Mirror. Current and Voltage References, Band gap Reference.

CMOS Operational Amplifiers

Design of CMOS Op-Amps, Compensation of Op Amps, Design of Two-Stage Op-Amps, Common-mode Rejection Ratio (CMRR), Power- Supply Rejection Ratio (PSRR), Cascode Op-Amps, and Characterization Techniques of OP-Amps.

Mixed Signal Design Fundamentals

Design of MOS Comparators, Data Converter Fundamentals, Digital-to-analog Converters, Analog-to-Digital Converters, Switch Capacitor Circuits, Phase locked loops, Techniques of Analog Layout.

References:

1. Allen, P. E., & Holberg, D. R. (2004). CMOS analog circuit design. Oxford University Press.
2. Razavi, B. (2002). Design of analog CMOS integrated circuits. Tata McGraw-Hill.
3. Baker, R. J., Li, H. W., & Boyce, D. E. (2002). CMOS circuit design, layout, and simulation. PHI.
4. Van de Plassche, R. J. (2003). CMOS integrated analog-to-digital and digital-to-analog converters. Springer.

Weightage: Continuous Assessment: 40%, End Semester Examinations: 60%
Assessment Methodology: Quiz (5%), Assignments (10%), Review of Question Papers (IES, GATE, SSC Questions) (20%), Projects (20%), Flipped Class (5%), Internal Examinations (40%).

	CO description	PO Mapping	PSO1	PSO2
CO1	Describe the integration of analog and digital subsystems in electronic system design	-	-	-
CO2	Analyze and design CMOS analog and digital building blocks using device-level models.	PO3(3)	3	3
CO3	Develop and simulate mixed-signal circuits simulation tools for real-time applications.	PO1(3)	3	2
CO4	Evaluate the analog and digital sub systems performance parameters through lab experiments..	PO1(3) PO(2)	2	3