JAYA ENGINEERING COLLEGE
THIRUNINRAVUR 602024

SUB CODE/SUB NAME - EC2354 VLSI DESIGN

ALL POSSIBLE 16 MARK QUESTIONS

UNIT-I

1. Explain in detail with a neat diagram the steps involved in IC fabrication process.
2. Explain the C-V and I-V characteristics in detail.
3. With a neat diagram discuss in detail about the DC transfer characteristics of CMOS.
4. Differentiate p-well CMOS process with n-well CMOS process. Explain n-well process.
5. Explain the gate, source/drain formation and isolation steps of CMOS fabrication process.
6. Explain in detail the Silicon On Insulator (SOI) process with a neat sketch.
7. Discuss in detail with a neat layout, the design rules for CMOS inverter.
8. Explain briefly about CMOS process enhancements.
9. Explain in detail the body effect and its effect in NMOS and PMOS device.
10. Derive an expressions for V_{in} of a CMOS inverter to achieve the condition $V_{in} = V_{out}$. What should be the relation for $\beta_n = \beta_p$.
11. Explain various issues in Technology-CAD and manufacturing in detail.

UNIT-II

1. Discuss in detail about the various delay estimation models.
2. Explain the static and dynamic power dissipation in CMOS circuits with necessary diagram.
3. Explain in detail about the threshold voltage equations.
4. (a) Discuss the mathematical equations that can be used to model the drain current and diffusion capacitance of MOS transistor.
   (b) Give a brief note on logical effort and transistor sizing.
5. Give a brief account on design margin.
6. Explain the different reliability problems related to the design of reliable CMOS chips.
7. Give a brief note on constant field scaling and voltage field scaling.

8. With necessary equations, explain in detail about:
   (a) Short channel
   (b) Narrow channel.
9. Draw the equivalent circuit structure of various MOSFET device models in SPICE.
10. Explain in detail about device models and device characterizations.

UNIT III

1. Briefly discuss about the classification of circuit families and comparison of the circuit families.
2. Write the basic principle for low power logic design.
3. Explain in detail about pseudo-nMOS gate with neat diagram.
4. Obtain the concept of static and dynamic CMOS design.
5. Compare the sequencing in traditional and skew-tolerant domino circuits.
6. (a) Implement Y= (A+B)/(C+D) using the standard CMOS logic.
   (b) Implement NAND gate using pseudo-nMOS logic.
7. (a) Implement D-lip-flop using transmission gate.
   (b) Implement a 2-bit non-inverting dynamic shift register using pass transistor logic.
8. Explain in detail about the pipeline concepts used in sequential circuits.
9. Explain the methodology of sequential circuit design of Latches and Flip-flops.
10. Explain the problem of metastability with neat diagram and expressions.

UNIT IV

1. Discuss the need for testing and explain about the silicon debugging principles.
2. Explain about the manufacturing test principles.
3. Describe the principle and application of Built-In-Self test.
4. Explain in detail about the sequence of scan-based technique.
5. Explain the Design For Testability (DFT) concepts.
6. (a) Explain the various fault models and also explain how to detect a stuck at fault with example.
   (b) Explain the various logic verification principles.
7. Explain the method of boundary scan test in detail.

UNIT V

1. Write about the basic elements of Verilog HDL.
2. Write down the Verilog HDL code for basic adder and subtractors.
3. Discuss about the data types and operators in Verilog HDL.
4. Write down the Verilog HDL code for Ripple Carry Adder, Encoder and Decoder.
5. Write down the Verilog HDL code for multiplexer and de-multiplexer.
6. Write a Verilog HDL for a positive edge-triggered D flip-flop. Using that implement an 8-bit shift register in structural model.
7. Design and develop HDL project to realize the function of priority encoder using structural modeling.
8. Write a data flow model and behavioral level Verilog HDL program for two input comparator circuit.
9. Explain the following in VERILOG with a suitable example.
    (i) Timing control and Conditional statements.
    (ii) Behavioral and Gate level modeling.
10. Write the VERILOG code for
    (i) Equality detector.
    (ii) D-Latch.