JAYA GROUP OF INSTITUTIONS – THIRUNINRAVUR.

6TH Semester – B.E. / B.Tech.

INTERNAL ASSESSMENT-II (Model Examination – II)

Sub. Title : **VLSI Design** Date : **05.03.2015**
Sub. Code : **EC2354** Branch : **ECE**
Duration : **180 Minutes** Max. Marks : **100**

Part A – (10 x 2 = 20)

Answer all questions

1. What is Bubble pushing?
2. Draw a pseudo- nMOS inverter.
3. What are the advantages of transmission gate?
4. Define sequencing overhead.
5. Define metastability.
6. What is the need for testing?
7. What are the various fault models?
8. What is Ad-hoc testing?
9. What are the various scan-based approaches?
10. What is BILBO?

Part B – (5 x 16 =80)

Answer the questions as per the choice.

11. (a) (i) Explain about pseudo – nMOS gates with neat diagram in detail. **(8)**

(ii) Discuss in detail the characteristics of CMOS transmission gate. **(8)**

Or

(b) (i) Explain about CVSL with neat diagram in detail. **(8)**

(ii) Describe the basic principle of operation of dynamic CMOS, domino and NP domino logic with neat diagrams. **(8)**

12. (a) Discuss in detail about various circuit designs of latches and flip-flops. **(16)**

Or

(b) With the help of relevant diagrams, describe sequential dynamic circuits in detail. **(16)**

13. (a) What is synchronizer? Explain the problem of metastability with neat diagrams and expressions. **(16)**

Or

(b) (i) Discuss about logical verification principles in detail. **(6)**

(ii) Explain the principle of silicon debugging. **(10)**

14. (a) Explain the manufacturing test principles in detail. **(16)**

Or

(b) Describe the ad-hoc and scan based approaches to design for testability in detail. **(16)**

15. (a) With the essential circuit modules, explain in detail the BIST and BILBO technique. **(16)**

Or

(b) Discuss with brief notes the various approaches involved in boundary scan techniques. **(16)**