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JAYA GROUP OF INSTITUTIONS – THIRUNINRAVUR.

6TH Semester – B.E. / B.Tech.

INTERNAL ASSESSMENT-I (Model Examination – I)

Sub. Title	**: VLSI Design**	Date	**: 27.01.2015**
Sub. Code	**: EC2354**	Branch	**: ECE**
Duration	**: 180 Minutes**	Max. Marks:	**100**

Part A - (10 x 2 = 20) Answer all questions

1. What are the different MOS layers?
2. Determine whether an NMOS transistor with a threshold voltage of 0.7V is operating in the Saturation region if $V_{GS} = 2V$ and $V_{DS} = 3V$.
3. When the channel said to be pinched off?
4. What are the different process techniques to enhance the performance of CMOS transistors?
5. Write down the equation for describing the channel length modulation effect in NMOS transistors.
6. Write the expressions for the logical effort and parasitic delay of ' n' input NOR gate.
7. Define Elmore delay.
8. What are the two components of power dissipation?
9. What is CMOS latch up? How it can be prevented?
10. Why does interconnect increase the circuit delay?

Part B - (5 x 16 = 80) Answer the questions as per the choice.

11.(a) (i) Explain the operation of enhancement nMOS transistor. **(8)**

(ii) Derive an expression for drain to source current (I_{ds}) equation for MOSFET. **(8)**

Or

(b) (i) Explain the non-ideal effects of MOSFET in detail. **(8)**

(ii) Explain the C-V characteristics in detail. **(8)**

12. (a) (i) Draw and explain the DC transfer characteristics of a CMOS inverter with necessary conditions for the different regions of operation. **(8)**

(ii) Discuss in detail with a neat layout, the design rules for a CMOS inverter. **(8)**

Or

(b)(i) Explain the gate, source/drain formation and isolation steps of CMOS fabrication process with neat diagrams. **(8)**

(ii)Give a brief note on the different process techniques to enhance the performance of CMOS transistors. **(8)**

13. (a) (i) Explain the principle of SOI technology with neat diagrams. Discuss its advantages and disadvantages. **(8)**

(ii) Give a brief note on manufacturing issues and technology- related CAD issues. **(8)**

Or

(b) (i) Discuss in detail about the resistive and capacitive delay estimation. **(8)**

(ii) Give a brief note on logical effort and transistors sizing. **(8)**

14. (a) (i) Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. **(10)**

(ii) Define: (i) Parasitic delay. **(3)**

(ii) Branching effort. **(3)**

Or

(b) (i) Explain the different reliability problems related to the design of reliable CMOS chips. **(10)**

(ii) Give a brief account on design margin. **(6)**

15. (a) (i) Explain in detail about (a) Constant field scaling. **(5)**

(b) Constant voltage scaling. **(5)**

(ii) Obtain an expression for level 2 model equation of MOSFET in SPICE. **(6)**

Or

(b) With necessary equations, explain in detail about

(i) Short channel effect. **(8)**

(ii) Narrow channel effect. **(8)**