6th Semester – B.E. / B. Tech
Model Exam-III

Sub. Title : VLSI DESIGN
Sub. Code : EC2354
Duration : 3 Hours

Date : 8.04.2015
Branch : ECE
Max. Marks: 100

Part A - Answer all the Questions: (10 x 2 = 20)

1. Discuss the various isssues in technology CAD
2. Define lamda layout rules
3. What is meant by design margin
4. How do you define the term device modeling
5. List the various power losses in CMOS circuits
6. Enumerate the features of synchronizer
7. List the basic types of CMOS testing
8. What is meant by logic verification
9. Give the comparison between structural and switch level modeling
10. What are gate primitives

Part B –Answer as per the Choice: (5 x 16 = 80)

11(a) (i) Explain about layout design rules (8)
(ii) Explain about CMOS process enhancement in SOI (8)

OR

11(b) Explain the fabrication process of twin tub (16)

12(a) (i) Explain the different factors that affect the reliability of CMOS chip (8)
(ii) Discuss the principle of constant field and lateral scaling. Write the effects of the above scaling method in the device characterization(8)

OR

12(b) (i) Give a brief account on design margin(8)
(ii) Give a brief note on logical effort and transistor sizing(8)

13(a)(i) Describe the different method of reducing static and dynamic power dissipation in CMOS circuits (8)
(ii) Explain the Domino and dual rail domino logic families with neat diagram(8)

OR

13(b) (i) Draw and explain about the conventional CMOS, pulsed and resettable latches (8)
(ii) Write a brief note on sequencing dynamic circuits (8)

14 (a) (i) Explain the following
1. Silicon debug principles (8) 2. Fault Models (8)

OR

14(b) (i)Describe the principles and application of Built in self test (8)
(ii)Explain how to detect a stuck at fault with example (8)

15(a) (i)Draw an active high 2/4 decoder using NOR gates and write the verilog gate level description(8)
(ii)Describe the three ways of specifying delay in continuous assignment statement(8)

OR

15(b) (i)Write a data flow modelling for 4:1 mux(8)
(ii)Explain the different timing control available in verilog(8)